

New Inverter Layout and DC Link Capacitor Integration for Increased System Density and Performance

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Abstract - A new Inverter/DC Link Capacitor approach to integration could facilitate 105°C coolant operation and greatly increase power density at elevated temperatures.

I. Introduction

The power inverter systems integrated into an under-the-hood traction drive require capacitors capable of carrying substantial high frequency currents to minimize the impact of high ripple currents on high energy density storage devices like super-capacitors and battery packs, load-sensitive power sources such as fuel cells, and to ameliorate the impact of switching voltage transients on power semiconductor devices such as IGBT's and PowerFET's. Additionally, the inverter semiconductor devices themselves require cooling and an efficient topological layout to provide high volumetric power density.

Aluminum Electrolytic capacitors are prevalent in today's DC bus filter (or DC Link Capacitor) applications for inverters, especially lower voltage systems in smaller HEV drivetrains and small electric vehicles, and along with standard, packaged semiconductor devices, are typical for the active inverter electronics design. These combine for good energy and capacitance density, reasonable performance and low component cost, but at a price of stringent cooling requirements and sometimes significant volumetric inefficiency. This is partly because electrolytic capacitors have fundamental material limitations, which prevent their use at temperatures exceeding +70°C when de-rated for even medium-term reliability and for operating, or even short duration voltages over 400 VDC¹. The electrolytic capacitor's Effective Series Resistance (ESR) is high and rises dramatically at low temperatures, limiting its ability to absorb and deliver energy at the low ambient temperatures frequently experienced in a large portion of the nation. This limits the overall performance and power density of the inverter both directly due to the capacitor and indirectly as the semiconductors are affected by the ESR and the Effective Series Inductance (ESL) due to packaging inefficiencies.

Recent efforts by many in the industry to substitute polymer film capacitors, with higher voltage ratings of 500 – 1000 VDC, for electrolytic capacitors in inverters

have used banks of parallel and series connected conventional cylinder-shaped, or flattened cylindrical sections, of smaller capacitors to form a complete module in order to achieve the required voltages to distribute the current flow, or achieve the desired amount of total capacitance required. This approach severely limits the designer's ability to remove heat generated by the capacitors and interconnects, limits the choices on locations for the capacitor bank, increases the ESR, increases the total volume needed, and adds considerable complexity and cost. Similar packaging issues remain a problem for typical electrolytic capacitor form factors as well but are increased with the film solution due to the natural disadvantage that film capacitors have in terms of capacitance density. In fact, universally, it has been found that, unless a capacitor has been carefully designed for long-term operation at elevated temperatures, high-temperature failures observed in commercially available components will most often be related to the individual devices' packaging and contacts technology, rather than the dielectric materials employed².

Consequently, it is the heat dissipation of the DC Link Capacitor bank while it is under the load of 100 – 400 Arms ripple current, which is rapidly becoming one of THE design limiters for the HEV and PHEV transportation inverter solutions available to industry today.

One of the more significant issues preventing the largest reduction in system volume, weight, and cost in the HEV and PHEV traction drive inverter systems envisioned for a next generation of these vehicles is the requirement of currently available polymer film, such as polypropylene (PP) film, capacitor technology to be cooled so that the hot spot temperature of the capacitor, while under load conditions, is lower than 85°C for long term reliability³. In order to achieve this condition, the capacitor solution must be cooled below that point even as it is self heating due to ripple current pass-through. In a traditional film capacitor form factor, such self heating can result in a 25 - 50°C rise from ambient surrounding temperature⁴. This can necessitate coolant temperatures of between 35 - 50°C in order for the film capacitor solution to remain reliable under full current rating conditions or 50 -70C if much larger than necessary capacitors are used and subsequently de-rated.

A typical system design engineering approach to this self heating and subsequent cooling requirement need of PP film capacitors is to allow the temperature of the hot spot to rise above the accepted 85°C long term reliability temperature point and distribute the inverter's DC Link ripple current across a larger number of PP film capacitors. This technique, known in the industry as "de-rating" can allow the temperature to rise within the capacitor to as much as 95 - 105°C and still remain a long term reliable solution but at reduced maximum total current allowed through any individual capacitor section⁵. However this technique still requires coolant systems delivering 50 to 70°C because the "more capacitor sections in the bank" solution does nothing to help the temperature rise expectation of any individual capacitor section per unit of RMS current (temperature rise is proportional to RMS current squared). And a cooling system of this temperature level means that a separate cooling line, infrastructure, and power drain will reduce the HEV or PHEV's overall drivetrain efficiency due to added weight and volume, to say nothing of costing more than desired. It also requires many more PP film capacitor sections in order to distribute the current. This adds cost, volume, and weight and is not desirable.

Some would argue that a 70°C coolant line is typically needed for IGBT thermal management however, without the necessity of special capacitor cooling, the cost/performance value proposition can take on an entirely different look if sub-105°C cooling lines can be eliminated.

Additionally, even if the inverter remains cooled at temperatures of 70 – 80°C, the spacing of capacitors inside the Power Electronic Module can be greatly reduced if allowable temperatures were not constraining in the capacitor design.

A further enhancement to this solution is to use High Temperature PP film such as High Crystalline PP film. Such film is described to have increased high temperature characteristics which may make it usable up to 115 or even 125°C⁶. This would allow the possibility of current distribution across a somewhat smaller number of sections than that required by standard PP film or might allow a somewhat higher coolant temperature for a single capacitor. However, such PP film material capacitors of this design would still require a coolant temperature of 65 to 90°C. This is still too low to use an available 105°C ICE coolant for efficiency and lower cost and the voltage limitations of such film at elevated temperatures may make them unsuitable for many powertrain applications.

What is required is a capacitor design which can operate reliably using 105°C coolant. Such a design would achieve the lowest possible weight, volume, and

system cost if it utilized relatively inexpensive film capacitor materials such as PP.

And if such a design did exist, the volumetric efficiency of the inverter could additionally be increased if the semiconductor topology of the devices could be integrated into or around a successful capacitor design without the worry of thermal runaway.

Lastly, the combination of the successful capacitor design and the optimization of the inverter semiconductor topology could, in fact, actually further increase the total inverter system performance if electrical and/or cooling characteristics might actually be enhanced by the integration.

This identifies the goal of the innovative new technical approach by SBE Inc.: To create a 105°C coolant capable capacitor design which exhibits long term reliability and enables greatly increased volumetric density and electrical performance of the entire inverter system while lowering cost.

II. Innovative Approach

The wound-film capacitor ring geometry shown in figure 1, and recently introduced by SBE Inc. to industry, has been demonstrated to greatly increase capacitance density for film capacitors⁷.

Terry Hosking, SBE VP Technology, invented the technique of locating a load (i.e. electronic, semiconductor package, etc.) inside the center hole of the annular capacitor for the specific purpose of reducing the ESL (inductance) of an application, which uses the capacitor and has been issued US patent number 7,289,311. One such application of this is the inverter and DC Link Capacitor relationship.

Over the past year, SBE has worked on joint research and development involving installing inverter semiconductors in the hole of the annular form factor film capacitor with the US DoE Oak Ridge National Labs (ORNL) and observed excellent initial improvement⁸. Concept designs that have been jointly investigated by SBE and ORNL suggest that simple cooling could be implemented, and that significantly greater volumetric power density could be achieved, if an optimized design of capacitor and unpackaged semiconductors were assembled in the hole on a bonded substrate.

However, in order to achieve the desired results, we must understand the following critical elements:

1. what the thermal effect on the DC Link capacitor will be under the proposed load conditions

2. what are the various cooling techniques possible
3. what will be the net effect of having the semiconductor die topology in the center, both electrically and thermally.

The process of capacitor analysis is complicated by the relationship between various geometric and material properties. The following parameters are interdependent and any final capacitor design solution will involve “trade-offs” between them:

- a) Film thickness: energy density + thermal conductivity
- b) Metallization thickness: thermal conductivity + losses
- c) End connection configuration: losses + thermo-mechanical limit
- d) Package aspect ratio: energy density + thermal expansion + thermal mismatch

From the preliminary design and analysis already performed by SBE Inc., it is believed that the optimum thermal and volumetric efficiency will come from locating the inverter semiconductors inside the hole of the inverter.

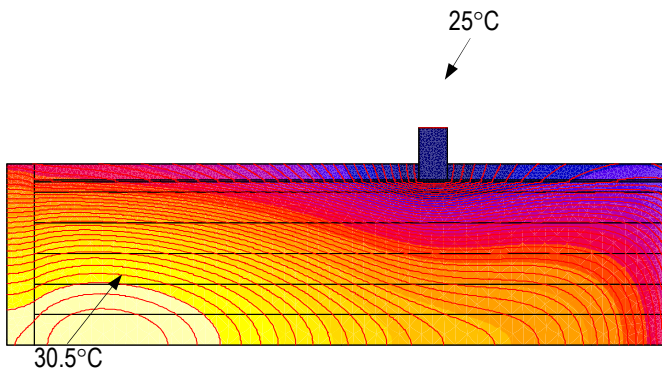


Figure 1 - Thermal profile for an early prototype annular form factor capacitor with a symmetric contact located outside the mean radius⁹.

This arrangement represents the best ratio of cooling plate surface area to current density within the capacitor and subsequently the lowest possible temperature rise under the conditions.

Using the coaxial magnetic properties of symmetrically distributing the high current IGBTs, either inside the hole or around the outer perimeter, also reduces what can become significant “eddy current” effects on the overall capacitor and, left unmitigated, will become the system current limiter for the inverter.

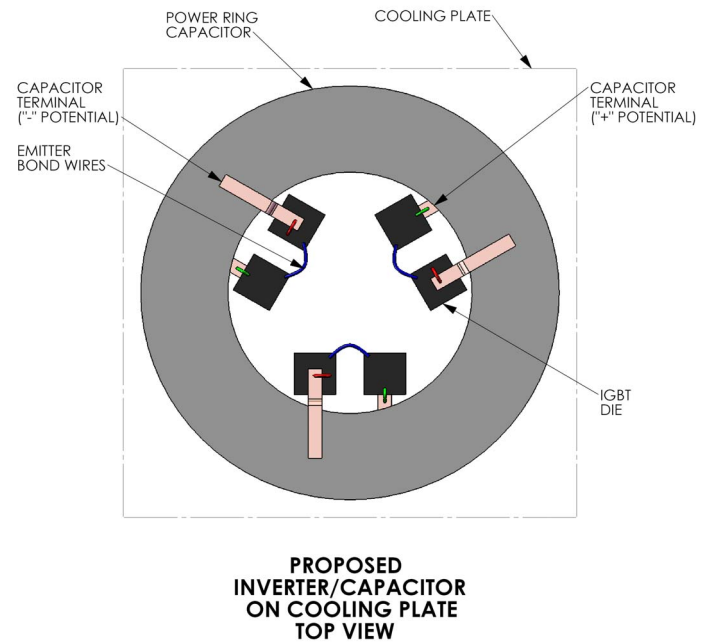


Figure 2 – From SBE Provisional Patent application Filed November 1, 2007¹⁰

SBE Inc has conducted preliminary tests and performed parallel modeling of this type of current distribution under room ambient conditions for a 240 Arms PHEV type ripple current application¹¹.

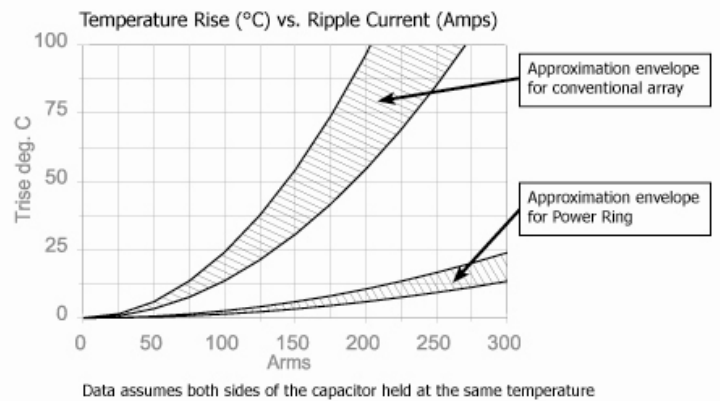


Figure 3 – Temperature Rise of Annular DC Link vs. Conventional Array for the 25°C example.

In order to be successful for the goal of long term reliability using the 105°C ICE coolant temperature or other inverter dense temperature conditions, we believe that a temperature rise of less than 10°C will be required while operating at maximum rated operating

temperature. This would establish a maximum hot spot temperature of less than 115°C within the capacitor. Data obtained in SBE’s SBIR Phase I program for the DoE, indicates that the reliability cross-over point for both MPP and HCMPP film is 125°C at the internal hot spot temperature. Our recently funded DoE Phase II, will generate specific reliability data for high density inverter applications using elevated temperatures and coolant loops.

We are not concerned about the fact that the most reliable implementation might also require some film capacitor current de-rating and consequently additional film capacitance to reach the desired PHEV and EV inverter ripple current requirements. The reason for this is that the volumetric efficiency of the annular form factor is up to 35% more efficient than a corresponding capacitor bank solution by design¹², so some additional capacitance for this purpose will have a minor effect on total volumetric efficiency vs. existing designs, especially when the possible complete elimination of the additional cooling loop is factored in or the much greater flexibility of component placement within the inverter is enabled.

Similarly, as we finalize the understanding of the temperature affects about the DC Link Capacitor in the annular form factor, similar information must be generated from semiconductor thermal analysis of inverter switching semiconductors located within the hole and co-located on the same cooling plate. The authors have performed previous work on understanding the cooling requirements of semiconductors under power in the center hole of an annular form factor DC Link Capacitor¹³, however detailed thermal analysis has not been performed yet. Research partners in this area are solicited

Also the resulting increase in volumetric power density with an optimized heat exchanger and cooperatively simulated thermal analysis and optimized modeling of the capacitor and semiconductors acting in the inverter environment have not yet been performed. Break-through advances in this multi-disciplinary area are possible.

In theoretical analysis of understanding the current flow in a large distributed capacitance where single element analysis is no longer sufficient to describe the self heating properties (i.e. an annular form factor), the we have already demonstrated that in order to maximize the total current handling capabilities of the capacitor, as equal currents as possible need to be flowing through the capacitor¹⁴.

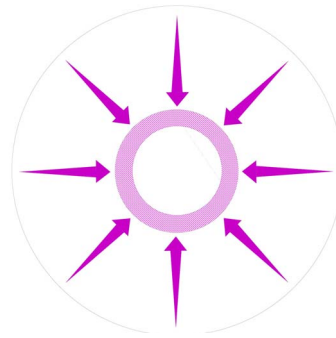


Figure 4 – Distributed Current in an Annular Ring Form Factor Capacitor¹⁵

This is because the maximum current rating of the device under long term conditions will result from identifying the worst case hot spot temperature and establishing current limits to keep this hot spot below the point where permanent heat damage will occur to the PP film in that area.

The optimum designs for a switching semiconductor layout of devices within the hole will take best advantage of this uniform current flow within the DC Link Capacitor to best reduce temperature rise under full current load conditions and as mentioned previously take symmetrical advantage of magnetic effect mitigation.

One might consider that if the hole of the capacitor needs to become too large to accommodate the necessary power semiconductors then the resulting circle of the annular form factor capacitor might need to become too large for the necessary capacitance of the DC Link. However, geometry is helpful in this regard since a reasonably large center hole can be created without great loss of capacitance of the remaining ring due to the volumetric formula of:

$$\pi r^2 w$$

Where r is the radius of the capacitor area and w is the width of the capacitor film. A reasonably large portion of the total radius of the annular form factor capacitor can be removed for electrical use and still leave useable capacitance. As an example, 50% of the radius could be left available for electrical use and the corresponding reduction of capacitance would only be approximately 25%. Since the authors have calculated that the annular form factor shape results in up to a 35% increase in volumetric capacitor efficiency vs. the currently used capacitor banks in many HEV and proposed PHEV/EV inverters, it is quite possible that the power electronics of the proposed inverter could be completely contained within the “underutilized space” of today’s inverter capacitor banks.

In summary, the annular form factor Inverter/Capacitor enabled by this innovative approach presented, could simultaneously provide a number of technical advantages over competing approaches, including:

1. High current handling capability due to the large surface contact area for cooling and low internal heat generation by optimized design.
2. High temperature capability in the 105°C coolant regime, or elevated internal inverter temperatures using MPP as the dielectric film with known long-term reliability.
3. The highest possible current capability by specifically establishing the semiconductor topology in the center hole, or outer perimeter of the capacitor to equally divide the ripple current in the capacitor.
4. Electrical performance improvement as a result of the extremely low inductance (ESL) possible when using connections to the capacitor of short and symmetric design.
5. An overall reduction in volume vs. current design approaches with expected cost and weight reductions.

This innovative approach costs no more than current Film Capacitor technologies and is anticipated to cost less since it is of simpler capacitor construction and takes advantage of a simplified bus structure for the inverter.

The reason why the costs of the innovative new design should be less than the current film capacitor technologies employed, is because it uses the same type of PP film being used today in conventional designs. SBE has developed capacitor winding equipment which produces annular form factor capacitors at a speed of capacitance per minute equal to the conventional machines used to build smaller capacitor sections. Yet when the annular form factor capacitor comes off of the winding machine, it is already the appropriate size. Conventional film capacitor sections, however, have to be assembled into a large bank.

The impact of the successful discoveries outlined in this paper is significant. Currently the volumetric power density of inverters is greatly limited due mostly to the temperature limitations of the DC Link Capacitor for long term reliable use. As a result, significant complex cooling schemes are being attempted¹⁶ at a much higher cost than the industry can bear, and thus impeding substantial adoption of new alternative energy technologies in the marketplace.

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