

# Characterization of Equivalent Series Inductance for DC Link Capacitors and Bus Structures

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## Abstract

The equivalent series inductance (ESL) of the DC link capacitor and associated bus structure connecting to the switch module has important implications for optimization of electric vehicle inverters. In many cases, additional snubber (bypass) capacitors can be eliminated for sufficiently low ESL, thus reducing cost, weight and volume. This paper presents ESL measurements for realistic capacitor/bus structures using a practical method previously documented [1]. Supporting magneto-dynamic finite element analysis results are also presented and shown to agree quite well with the measurements. The measurement and simulation results demonstrate that a 1000  $\mu\text{F}$  600V Power Ring Film Capacitor™ has an ESL of approximately 3 nH with a properly designed terminal structure. The bus structure is shown to dominate the total ESL for both horizontal and vertical inverter topologies when using annular form factor film capacitors with an optimal terminal configuration.

## Introduction

The equivalent series inductance (ESL) presented to the switch terminals in an inverter circuit has significant implications for the design. The energy stored in this stray inductance must be managed during turn-off, in many cases using snubber (bypass) capacitors to avoid voltage overshoot problems. Traditionally, the “external” inductance contribution of the DC link capacitor and bus connection has been the dominant factor for overshoot. However, with an optimized capacitor/bus topology it is now possible to achieve external inductances on the same order as the internal inductance of the IGBT package.

Practical capacitor and bus structures have been designed and fabricated for both horizontal and vertical inverter topologies which can accommodate industry standard “six pack” IGBT modules. Inductance measurements at the IGBT terminals of the capacitor/bus arrangements are presented and discussed. The relative contributions of the capacitor and bus are unfolded and the latter is demonstrated to dominate the ESL. Simulation results for a 1000  $\mu\text{F}$  annular form factor capacitor are described and correlated with the ESL measurements of the same part. ***The results clearly demonstrate that a DC link capacitor inductance of approximately 3 nH can be achieved in practice with a total ESL of less than 20 nH presented to the IGBT terminals.*** A significant portion of the total ESL results from the input terminal geometry defined by the IGBT package.

## 1. Conventional Technology

Traditional film capacitors for DC link applications utilize a “can” or “brick” style package. The former typically have a height that is greater than the winding diameter while the latter are comprised of small windings arrayed in parallel. The normal terminal arrangement for “can” capacitors consists of two threaded studs located on the same end of the cylinder. For “brick” capacitors, planar tabs are provided to mate with a bus bar or connect directly to the IGBT terminals. A very good overview of ESL data for conventional form factor DC link capacitors is provided by Montanari et al [2] which reports values ranging from 10 nH to 65 nH depending on package configuration. Looking specifically at large values in the 1000  $\mu$ F regime, the use of an internal bus bar with a rectangular “brick” package can achieve a capacitor terminal ESL on the order of 20 nH. However, it is very important to note that additional inductance will be added to the capacitor loop by the addition of the interconnections to the IGBT module. Next generation annular form factor capacitors with a properly designed coaxial terminal structure can be used to realize inductances of less than 5 nH. When such a capacitor is combined with a low-inductance laminar bus structure, total ESL values below 20 nH can be achieved at the IGBT terminals.

## 2. ESL Measurements

A variety of techniques have been reported for measurement of capacitor ESL. For example, a step response method for electrolytic capacitors using a reference resistor in series has demonstrated by Tsang et al [3]. Similarly, a discharge approach based on a Rogowski coil current sensor is described by Montanari et al [2]. SBE has recently developed an improved ESL measurement using a ring-out method as reported previously [1]. This approach is simple to apply and requires only measurement of the capacitor voltage as the diagnostic. Furthermore, the SBE method can be used to measure with the capacitor deployed on a complete bus structure, which has a significant contribution to the total inductance.

The ESL measurement applies a fixed voltage to the DC link capacitor which is then discharged through a specially designed no-bounce switch installed at the location of interest on the bus structure. The resulting ring-out waveform provides the resonant frequency of the circuit from which the total inductance can be determined from the known capacitor value. The capacitor contribution to the total inductance can be unfolded based on the initial step in the discharge waveform. This voltage step results from the voltage divider created by the bus and capacitor inductances.

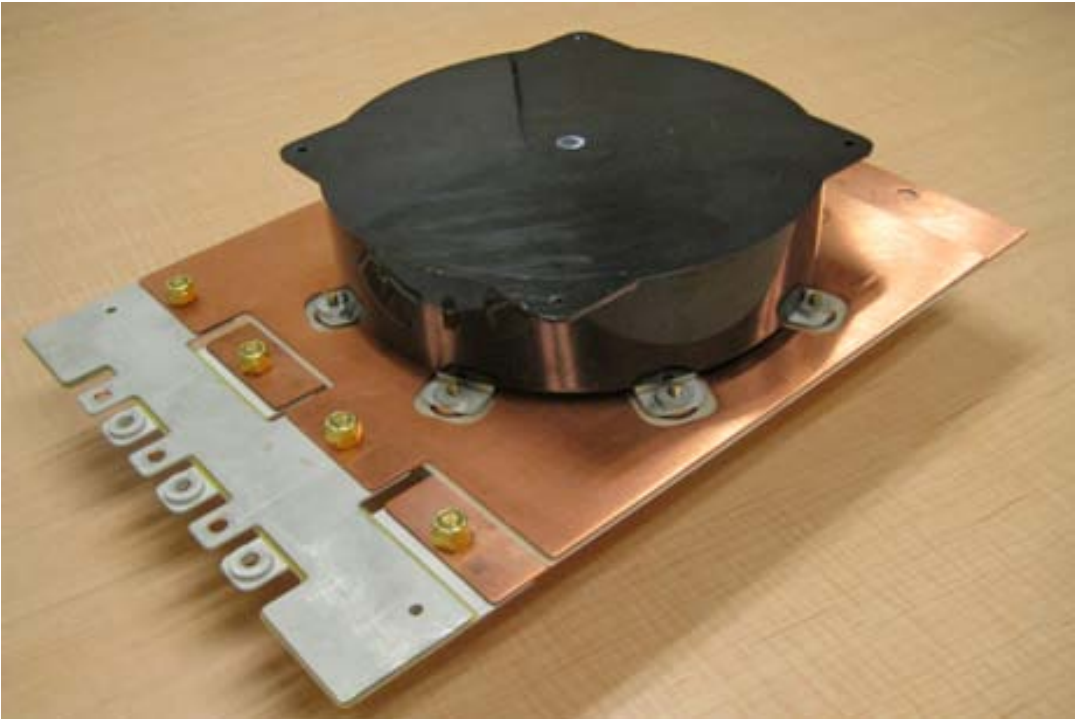
SBE has recently introduced a “universal” laminar bus that can be used for testing the 700D348 and 700D349 series DC link capacitors rated at 600 V with respective values of 1000  $\mu$ F and 500  $\mu$ F. Adapters are provided to facilitate integration of these capacitor/bus structures with standard three-phase IGBT modules to create a “horizontal” inverter test kit. A DC input connection is provided on the opposite end of the bus structure from the IGBT connection to provide the best exposure of the capacitor to the ripple current. While these laminar bus kits are not fully optimized to a specific application, they offer a reasonable basis for evaluation. The 1000  $\mu$ F and 500  $\mu$ F test kits fitted with adapters for mating with an Infineon HP2TM IGBT module are presented in Figures 1 and 2. A vertical topology using a 500  $\mu$ F capacitor and bus interfacing with a Danfoss E+™ module was also tested as shown in Figure 3. Note that the IGBT module was removed during the ESL test and that the DC input tabs are implemented on the opposite side of the capacitor from the switches.

The ESL of each capacitor/bus configuration was evaluated with the discharge switch located at each IGBT terminal pair. Note that the difference in ESL between the three IGBT terminal pairs is negligible for each of these geometries since the mean path lengths are nearly identical. The total assembly inductance and capacitor inductance are computed for each

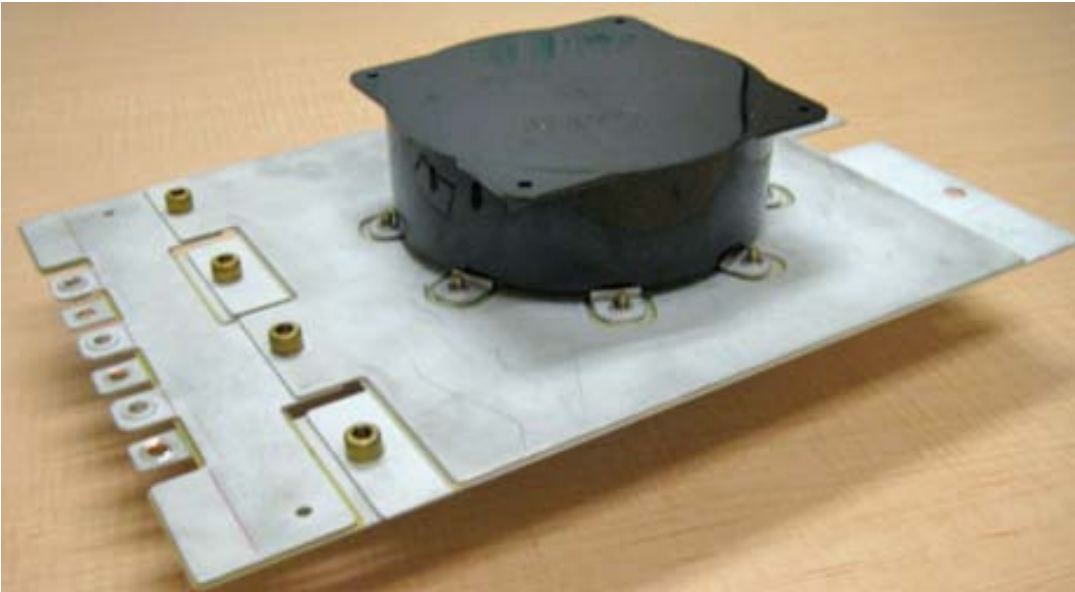
configuration in Table 1. The capacitor contribution to the total ESL is shown to be 15 to 20 percent of the total value.

Capacitance ( $\mu\text{F}$ )	Configuration	Capacitor ESL (nH)	Capacitor + Bus ESL (nH)
500	Horizontal	4.2	21
500	Vertical	3.79	18.5
1000	Horizontal	3.15	21

**Table 1.** Comparison of ESL measurements for different capacitance values and bus configurations.



**Figure 1.** Horizontal inverter configuration with a 1000  $\mu\text{F}$  capacitor.



**Figure 2.** Horizontal inverter configuration with a 500  $\mu\text{F}$  capacitor.

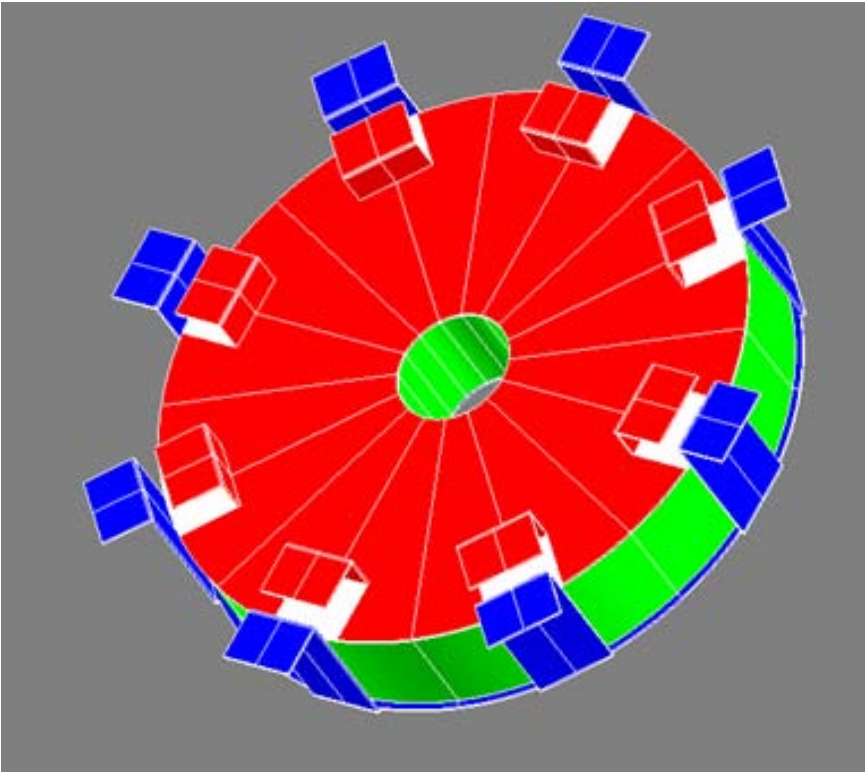


**Figure 3.** Vertical inverter configuration capacitor and bus.

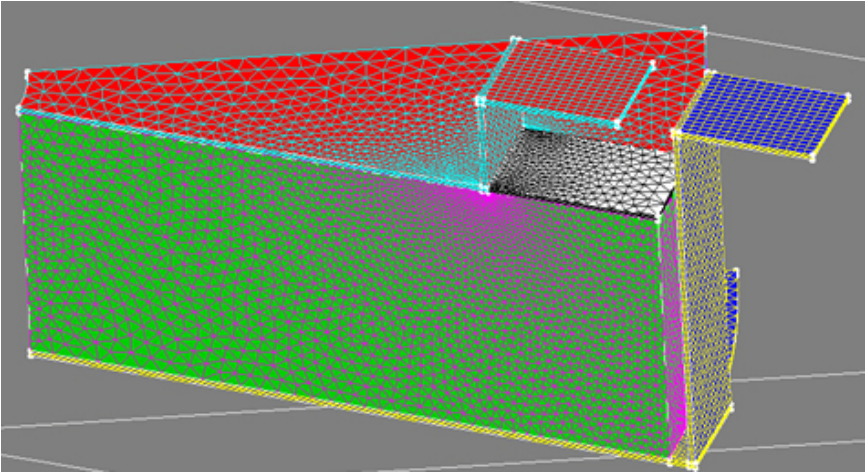
### 3. ESL Calculations

A magneto-dynamic analysis of the 1000  $\mu\text{F}$  capacitor structure used for testing was performed using the Flux3D™ software package [4]. The complete capacitor has a total of eight terminal pairs evenly spaced around the circumference as shown in Figure 4, but can be modeled assuming 1/16 symmetry. The reduced domain is presented in Figure 5 which also shows the mesh for the finite element analysis. Note that the capacitor winding dominates the series resistance and can thus be modeled as a bulk conductive region having an electrical resistivity of appropriate value. The copper terminals are much more conductive and the current distribution in this case will be dominated by the skin effect. For the selected analysis frequency of 20 kHz, the skin depth for copper is approximately 0.47 mm, which is significant relative to the terminal thickness. As such, the use of at least two second order “brick” elements over the thickness is essential to accurately model the current density distribution.

The problem is bounded by an infinite box to minimize the domain size while accurately representing the transition to the far field. The capacitor is driven by a one volt RMS signal applied between the inner and outer terminal feet. A calculation of the total current is performed by integrating the current density across the capacitor mid-plane, which then allows a computation of the impedance based on the known voltage drop. The resistive component of the impedance is unfolded by calculating the total losses in the structure such that the reactance and hence ESL can be determined. A value of 3.2 nH was computed using this method for the 1000  $\mu\text{F}$  capacitor, which agrees very well with the measured value of 3.15 nH.



**Figure 4.** Illustration of the complete 1000  $\mu\text{F}$  capacitor and terminal structure before applying symmetry assumptions.



**Figure 5.** Finite element analysis domain for 1/16 symmetry analysis of 1000  $\mu\text{F}$  capacitor.

## Conclusion

Measurements of various capacitor/bus structures have demonstrated that the ESL seen at the IGBT terminals is dominated by the interconnection when using properly designed annular form factor capacitors. While the capacitor ESL does have an effect, the contribution is typically around 20% of the total. The inductance values measured for a 1000  $\mu\text{F}$  capacitor have been validated by magneto-dynamic finite element analysis with the calculated and measured values agreeing to within two percent. Having obtained correlation between the measured and computed ESL values, the claim of significantly reduced DC link capacitor inductance has been substantiated.

These results are significant in that the total optimized bus/capacitor inductance presented at the IGBT terminals can clearly be reduced below 20 nH. The best traditional form factor DC link capacitors have inductances in this range without including interconnections. As such, a new low ESL regime is now possible where the external inductance seen by the IGBT is on the same order as the internal package inductance (approximately 15 nH). Operating in this regime can potentially reduce voltage overshoot and eliminate the need for snubber (bypass) capacitors which add cost, weight, and space to automotive inverter designs.

Another important aspect of the results is the surprisingly large contribution of the bus structure to the total ESL. Even with a favorable aspect ratio and minimal plate spacing, bus inductances well in excess of 15 nH were observed. A large portion of this inductance can be attributed to the tab configuration dictated by the IGBT input terminal spacing. The ripple current will be forced to the inner corners which define the closest distance between the tabs, thus creating the equivalent of two small wires. This has the dual effect of increasing inductance by enhancement of the magnetic field and causing local heating due to poor utilization of the tab cross section. Therefore, the reduced external ESL regime will have implications for IGBT input configurations and internal packaging which have traditionally been masked by the capacitor and bus bar.

## References

- [1] Sawyer, E. D., "Low Inductance – Low Temp Rise DC Bus Capacitor Properties Enabling the Optimization of High Power Inverters", PCIM 2010, Nuremberg, Germany, May 4-6.
- [2] Montanari, D., Saarinen, K., Scagliarini, F., Zeidler, D., Matti Niskala and Nender, C., "Film Capacitors for Automotive and Industrial Applications", CARTS Europe, September 2008.
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- [4] Flux3D™, Magsoft Corporation, 1 Fairchild Square, Suite 108, Clifton Park, NY 12065.