Optimized DC Link for Next Generation Power Modules

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Abstract

The market leaders in IGBT technology are now introducing next generation "six-pack" modules to enable increased power density and reduced cost for automotive traction drive applications. However, the potential gains offered by these modules can only be harvested using an optimized DC link with integrated capacitor/bus topology. Two integrated capacitor/bus solutions have been designed to support the new Infineon HybridPACK™ Drive [1] module with the lowest possible μF/kW ratio and minimized equivalent series inductance. Simulation and design results are presented along with third party testing data for a complete inverter.

1. Introduction

Next generation power modules for electric vehicle applications are targeting increased power density and efficiency to reduce drive train cost and weight. In order to fully exploit the capabilities of such modules, an optimized DC link comprised of high performance film capacitors integrated with a suitable bus structure is essential. This approach attacks the two critical factors that limit inverter power density, which are the ripple current per micro-Farad rating of the capacitor and the overshoot voltage across the IGBT switches during turn-off.

The power density of an inverter is traditionally limited by the DC link capacitance value required to safely source the ripple current demanded by the IGBT's during switching. *Using an annular form factor capacitor winding with low losses and low thermal resistance enables a new paradigm where capacitance is defined by the inverter control limit rather than Amperes per micro-Farad.* Note that this approach has recently been demonstrated for wind power where a reduction of DC link capacitance for a smaller μF/kW ratio facilitated fitting a 1MW inverter into a 500kW frame [2].

The DC input voltage for the inverter is constrained by voltage overshoot which results from energy stored in the parasitic inductance seen by the IGBT's during turn-off. This issue is best mitigated by reduction of equivalent series inductance (ESL) combined with intelligent gate control to safely increase the DC voltage closer to the IGBT limit. Annular form factor film capacitors can be "surface mounted" to the bus structure such that one bus conductor becomes a terminal of the capacitor. This approach eliminates redundant copper, thus reducing cost and weight while simultaneously reducing the ESL of the DC link capacitor. The use of optimized connections from the bus structure to IGBT module is essential to get the lowest possible ESL and hence overshoot [3].

The Infineon HybridPACK™ Drive (HP Drive FS820R08A6P2xx) [1] represents a new state-of-the-art IGBT module with new automotive EDT2 IGBT chip generation and a footprint

reduction of 30% relative to the last benchmark power module Infineon HybridPACK™ 2 with IGBT3 chip generation. Two optimized DC link capacitor/bus topologies have been designed specifically for the HP Drive to match the size reduction. A "horizontal" layout places the DC link capacitor in-line with the IGBT module. A "vertical" layout locates the capacitor/bus underneath the IGBT cooling plate to create a compact geometry. This paper discusses the design of both configurations in detail and inductance measurements are provided in addition to rating calculations based on practical cooling assumptions for a realistic drive cycle. Third party test results are presented for a full inverter using the "horizontal" DC link topology under steady state conditions.

2. DC Link Requirements

The Infineon HP Drive requires a DC link capacitor capable of the following:

$450V < V_{dc} < 550V$ $75Arms < I_{ripple} < 125Arms$ continuous $50^oC < T_{coolant} < 85^oC$

A capacitance of 500μF was specified with a life requirement of 10,000 hours subject to a typical automotive drive cycle. In order to match the module foot print, two annular form factor windings having a height of 32mm and outer diameter of 76mm were selected. Metallized polypropylene film was used for the dielectric to provide the best balance of cost and performance.

3. Horizontal Layout Design

The horizontal configuration DC link is presented in Figure 1a. Two 250μF annular film capacitor windings are directly integrated to a laminated bus structure and share a common "crown" terminal. Note that locating the DC input terminals to the cap/bus on the opposite side of the IGBT connections provides the best utilization of the capacitor and minimizes "current hogging". This configuration provides the shortest possible connection length from capacitor to IGBT inputs combined with "through-hole" connections to achieve the lowest possible ESL. The thermal profile for a single winding subject to 50Arms ripple with an 85^oC boundary defined on the capacitor case is presented in Figure 2a.

4. Vertical Layout Design

The vertical configuration DC link is presented in Figure 1b. The capacitor windings and "crown" terminal are identical to that utilized for the horizontal configuration, but the bus interface to the module is modified. While the optimal location of the DC inputs to the cap/bus relative to IGBT inputs is maintained, the ESL will be a few nH higher for this configuration since the path length is increased. A thermal finite element analysis was performed on a single winding for this case using the same methodology as per the horizontal layout. Note that in this case, the 85^oC boundary condition was applied to the bus to represent the effect of the IGBT cooling plate. The thermal profile for this case is presented in Figure 2b and the hotspot temperature rise is lower than the horizontal case for the same ripple current. While the ESL of this design is a bit higher than the horizontal layout, the current rating is significantly increased since bus and IGBT losses do not flow through the capacitor.

5. Inductance Measurements

The horizontal capacitor/bus test kit prototype was tested using the SBE ring-out method described previously [4]. This method indicates that the inductance at the IGBT inputs is 8.4nH. Independent measurements performed by Infineon on the optimized capacitor/bus similarly indicate a value of about 8nH. From a practical operating standpoint, Vce must be

limited to less than the Vces -40°C specification of the IGBT/diode chipset. While active collector gate clamping is implemented to limit Vce to <710V for the HP Drive, repetitive clamping circuit activation must be avoided to prevent damaging the TVS diodes, which can lead to uncontrolled short circuiting of the IGBT and module failure as a consequence. Higher stray inductances provide a larger overvoltage at turn-off which thus limits the maximum useable working voltage. Alternatively, higher Rg (gate drive resistance) can be adopted with the penalty of lower performance. The best utilization of working voltage can thus be achieved by minimizing the stray inductance.

Comparison of IGBT turn-off measurements between the optimized SBE 8nH capacitor/bus and a conventional 15nH capacitor were performed using the circuit in Figure 3a with the results presented in Figure 3b. The turn-off overvoltage was measured with and without the clamping circuit in order to determine the point of clamping circuit activation. At 500V working voltage, the SBE 8nH capacitor solution showed extremely low overvoltage and the clamping (overvoltage protection) was not active before 1000A. This indicates a usable transient current range up to 1000A at 500Vdc and the full switching speed of the power module can be utilized for working voltages of 500V to 550V. In contrast, the 15nH conventional capacitor testing results showed activation of the clamping circuit at above 500A at 500V. In order to safely operate at 500V with this capacitor, the switching speed has to be slowed down to avoid the risk of damage to the clamping circuit or the IGBT module.

These measurements clearly show that a low inductance capacitor/bus DC link is mandatory for applications that require high working voltages combined with full switching speed at high phase currents to achieve the lowest possible inverter power losses.

6. Inverter Testing Setup

An HP Drive module was supplied by Infineon along with the cooling plate, gate driver and micro-controller to support the inverter testing. The IGBT module was combined with an SBE 700A186 horizontal test kit DC link as shown in Figure 4. Note that an aluminum adapter block has been added to extend from the cooling plate to the capacitor case such that a thermal reference is defined. The capacitor was instrumented with thermocouples at the mid-plane of each winding located inside the core along with mirror image thermocouples on each winding end face. The core measurement is typically very close to the capacitor hotspot and the end face measurements provide a useful indication of the thermal gradient across the windings.

Additional thermocouple measurements were made at the following locations on the inverter:

1) IGBT module output tab for center terminal
2) Positive input to IGBT module on center tab pair
3) DC input tab on the capacitor/bus assembly
4) Aluminum cooling plate under capacitor case
5) Coolant inlet
6) Coolant outlet

Finally, the output of the RTD located on the IGBT module was recorded as a frequency signal that was later correlated to temperature using the relationship provided by Infineon. The complete test setup is presented in Figure 5. A static RL load was connected in a floating Wye across the IGBT module outputs and a Yokogawa WT1800^{TM} power analyzer was utilized to measure the efficiency of the inverter.

For the purpose of this paper the focus will be on a run to thermal equilibrium performed at 22^{o}C ambient temperature with a coolant temperature of 22^{o}C and a flow rate of 6.4 lpm.

The power analyzer output for this test is shown in Figure 6 and the inverter power was 35kW continuous. Note that the inverter was over modulating a bit as the system was adjusted to achieve a phase current of 75Arms without tripping the power supply.

7. Inverter Testing Results

With an inverter system efficiency level of 99% at the 35kW, 400Vdc, 8kHz light load condition, the new automotive EDT2 IGBT chip generation of the HP Drive strongly outperforms last IGBT generations. Further calorimetric based measurements at Infineon validated the recorded efficiency level of the Oak Ridge National Laboratory National Transportation Research Center. The statement, that the new EDT2 IGBT was developed for having an extended EV driving range, was thus clearly proven by this experiment. While the available test power is well below the capabilities of both the Infineon HP Drive and the SBE integrated cap/bus DC link, some very useful information was unfolded from the results. Consider the thermocouple data for the capacitor/bus assembly as compared to the simulation results using the 2D model described earlier with capacitor and capacitor plus bus losses as presented in Figure 7. There are two discrepancies between the measured data and the original design simulation; namely the total hotspot temperature and the thermal time constant. The former issue indicates that some small fraction of the IGBT chip and terminal losses are coupled to the bus via the module power tabs and flow through the capacitor. The latter issue demonstrates that there must be an additional thermal path from the bus to the ambient temperature.

The hotspot temperature can be deconstructed into a simple thermal resistance model as shown below:

$$\Delta T = P_{cap} \times R_{Tcap} + (P_{bus} + P_1) \times R_{Tbus}$$

Note that P_1 denotes the fraction of chip and terminal losses flowing to the IGBT power tabs that influence the capacitor/bus temperature. The simulation can be fitted to the test results by matching the hotspot temperature and thermal time constant. A parallel thermal resistance of 2.45°C/W from the bus to 22°C ambient provides a good match on the time constant. This is attributed to the DC input cables which provide strong coupling to ambient. Combined with an additional 1.96W of power supplied to each winding to account for P_1, the simulation aligns nicely with the data as shown in Figure 8. The relative contributions of the various mechanisms can be summarized in the same equation format as shown on a per winding basis:

$$4.87^{o}C = 0.27W \times 1.95^{o}C/W + (0.34W + 1.96W) \times 1.89^{o}C/W$$

Note that this corresponds to the red curve of Figure 8 after approaching equilibrium at 6000 seconds. The HP Drive design has significantly reduced the amount of heat added to the cap/bus from the power tabs as compared to conventional modules. This is achieved by the ultrasonic welded power tabs to the ceramics substrate.

Now consider scaling up to a more typical power level and coolant temperature for these products. Doubling the power to 70kW with the voltage fixed at 400Vdc requires that the capacitor ripple current and bus current increase by a factor of two such that the losses for both cases increase by a factor of four. The IGBT chip and terminal loss contribution will increase by a factor of 2.5 from the 35kW base case per Infineon calculations. Scaling to 85°C coolant will increase the electrical resistance of the bus conductors, capacitor electrodes, capacitor end spray, and capacitor terminals by the appropriate temperature coefficients. Infineon analysis indicates that the IGBT chip and terminal loss contribution will increase by approximately 6% going from 22°C to 85°C coolant. On a per winding basis, the

capacitor losses increase from 0.27W to 1.42W, the bus losses increase from 0.34W to 1.79W, and the IGBT chip and terminal contribution increases from 1.96W to 5.19W. The simple model predicts a temperature rise of 16^{o}C, which matches up nicely with the separately generated SBE capacitor simulation tool output as presented in Figure 9. This result can be readily utilized to generate a rating curve for the horizontal test kit on the basis of the capacitor and bus losses as presented in Figure 10.

Based on life testing results presented previously [5], a life of 10,000 hours can be achieved with a hotspot temperature of 100^{o}C operating at 400Vdc. As such, the capacitor can thus provide 10,000 hour life operating at 84^{o}C coolant and 70kW continuous power. The same scaling assumptions can be applied to further increase the power to 100kW at 400Vdc. Under this condition, assuming continuous operation, the 100^{o}C hotspot limit for 10,000 hour life can be maintained with 70^{o}C coolant. The HP Drive is intended for 50-150kW (peak) electric vehicle applications [1]. These scaling results indicate that the SBE horizontal test kit is fully capable of supporting high performance vehicle applications at the top end of the HP Drive power range. Given the long thermal time constant of the capacitor, peak power of up to 150kW can be readily managed for short durations as part of a realistic drive cycle. It is also important to recognize that the vertical capacitor/bus test kit offers even more capability since the bus bar is tied directly to the IGBT cooling plate. As such, the bus losses and any stray power from the IGBT chip and terminal losses will not flow through the capacitor. This translates to lower capacitor hotspot temperature rise, which will enable the vertical cap/bus kit to support 100kW continuous operation at 85^{o}C coolant or higher.

8. Conclusion

Horizontal and vertical configuration DC link capacitor/bus test kits have been designed and optimized for the Infineon HybridPACK™ Drive power module [1]. Independent measurements for the horizontal kit have confirmed an ESL of 8nH at the module inputs which is about 50% lower than can be achieved with conventional technology. This low inductance minimizes voltage overshoot and enables higher working voltages and faster switching speeds to achieve the best efficiency for the HP Drive. Third party testing of a complete inverter at the Oak Ridge National Laboratory National Transportation Research Center has provided critical thermal data for characterizing the performance of the horizontal test kit. Scaling these results to practical operating conditions indicates that this capacitor/bus can support 100kW continuous operation at 70^{o}C coolant and 400Vdc with a life of greater than 10,000 hours. The SBE 700A186 (500V and 500μF) therefore supports full utilization of the Infineon HP Drive for high performance EV applications. Similar performance can be achieved at even higher coolant temperatures using the vertical configuration test kit which allows even more compact topologies with only a minor penalty in ESL.

Acknowledgements

The authors wish to thank Mr. Larry Seiber and Mr. Steve Campbell at ORNL for their efforts in completing the inverter testing.

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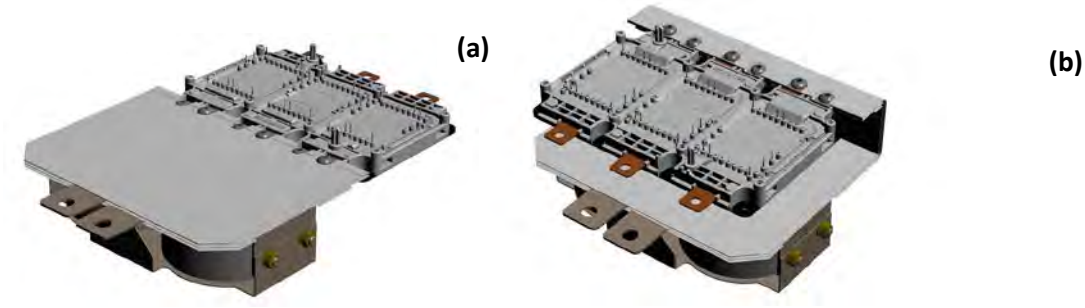

Fig. 1. Integrated capacitor/bus DC link for (a) horizontal and (b) vertical configurations

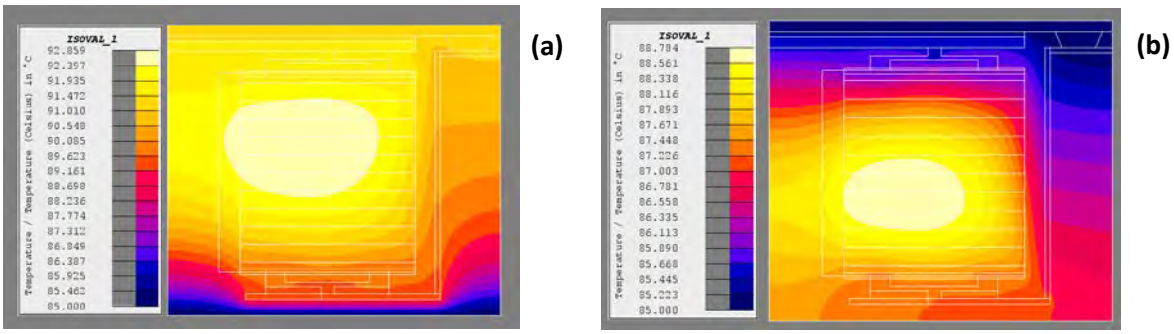

Fig. 2. Thermal profiles for single capacitor winding with (a) horizontal and (b) vertical configurations

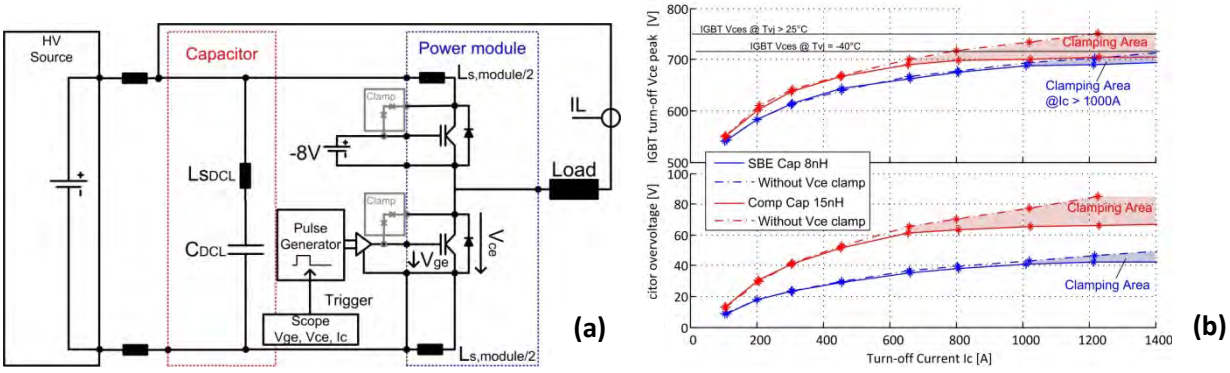

Fig. 3. Overshoot testing DC link capacitors at Infineon (a) test circuit, (b) turn-off overvoltage at 500Vdc working voltage.

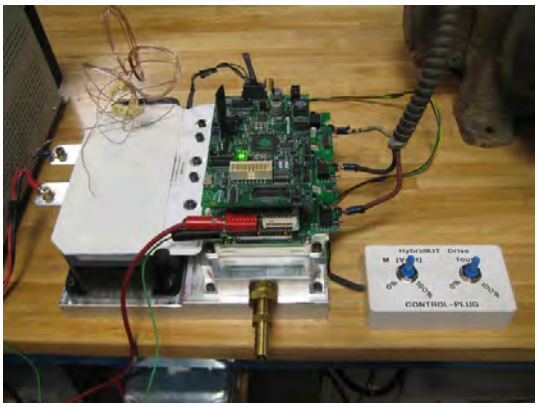

Fig. 4. Illustration of HybridPACK™ Drive and complete test kit HybridKIT Drive supplied by Infineon for inverter testing

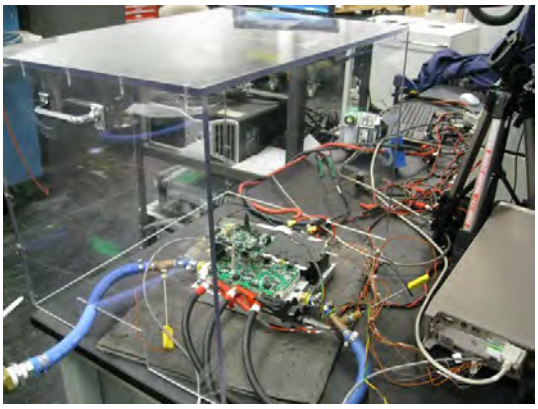

Fig. 5. Complete inverter test setup used at the National Transportation Research Center at Oak Ridge National Laboratory

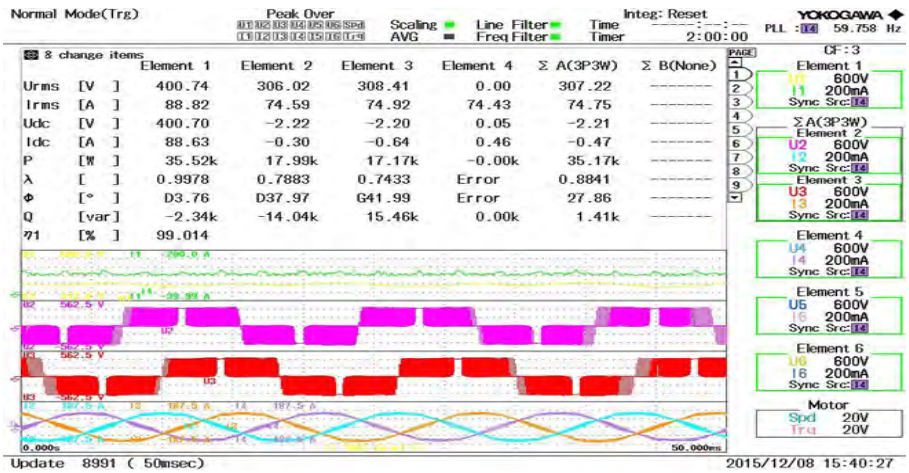

Fig. 6. Yokogawa WT1800™ readout for test run to equilibrium at 50ºC

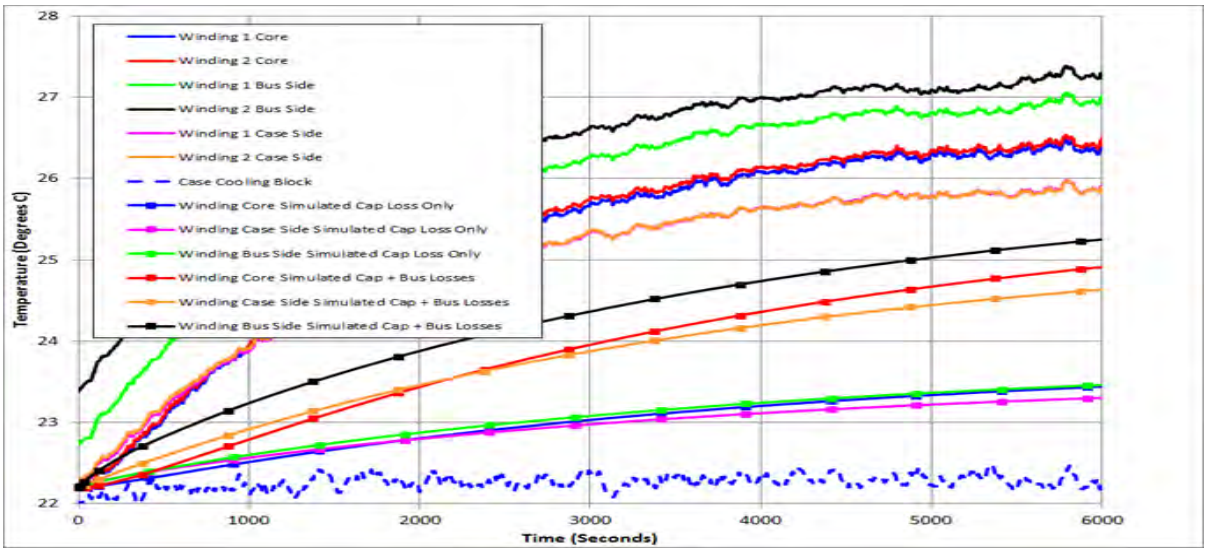

Fig. 7. Capacitor/bus thermocouple data as compared to original design simulation: Top six curves represent measured data, bottom curves show simulation with capacitor losses only, middle curves show simulation with capacitor and bus losses.

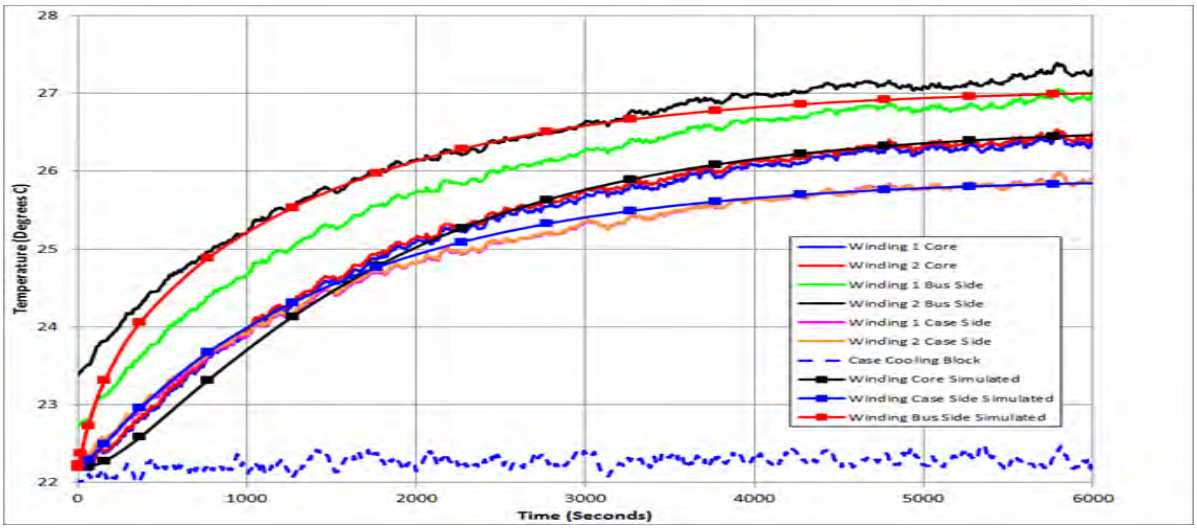

Fig. 8. Improved simulation accounting for additional thermal path and addition of IGBT losses to fit test data

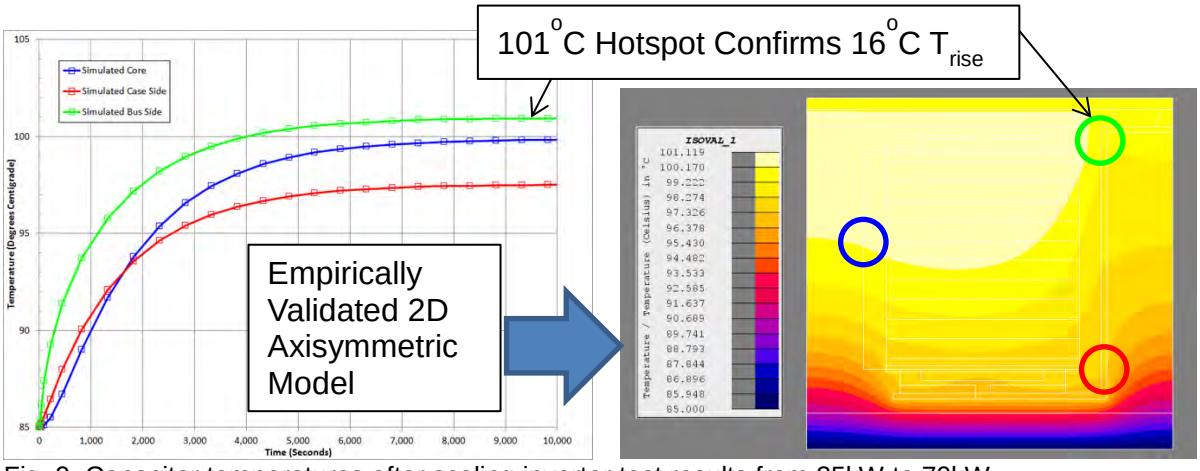

Fig. 9. Capacitor temperatures after scaling inverter test results from 35kW to 70kW

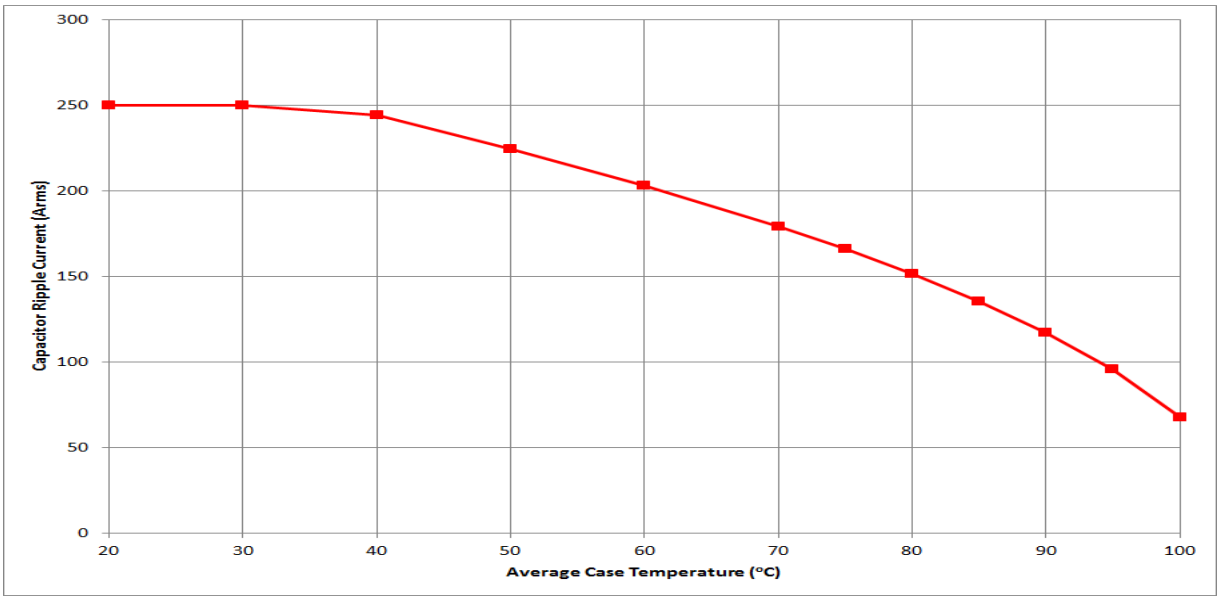

Figure. 10. Continuous current rating curve for the SBE 700A186 horizontal test kit based on inverter test data with capacitor and bus losses only