



# Motor & Drive Systems 2006

Miami, Florida – February 15-16, 2006



## Ring Form Factor Film Capacitors for Embedded Motor Controls

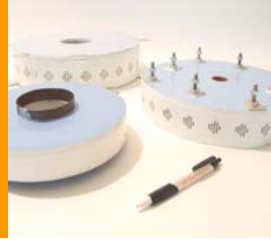
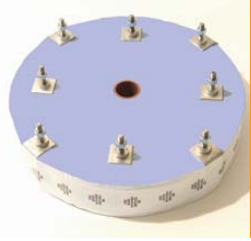
Consider an E-Drive Inverter located  
within the Motor Housing

Presented by:

Terry Hosking, VP of Engineering  
SBE, Inc.



# Consider E-Drive Inverter located within the Motor Housing

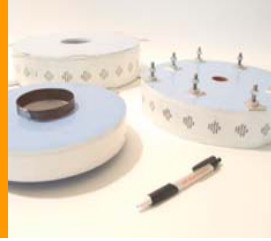
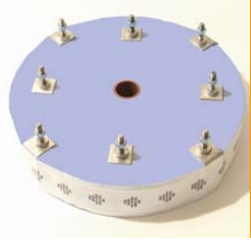


## ⚡ Advantages:

- ⚡ A more ideal Motor Form Factor for many applications
- ⚡ Smaller Volume/Lower Weight System
  - Higher Power Density
- ⚡ Electrical Efficiency Improvement Opportunity
- ⚡ The possibility to Reduce EMI



# Consider E-Drive Inverter located within the Motor Housing



## ⚡ Challenges:

### ⚡ Thermal Management

- More Cooling Capacity Needed

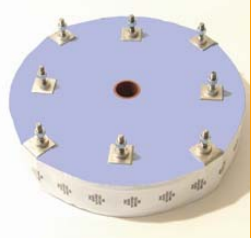
### ⚡ Sourcing Suitable Components

### ⚡ Round PCB Boards/Bus Structures are not “the norm”

### ⚡ DC Link Capacitor Assembly

Note: The concept of an embedded inverter is not presented as a unique idea





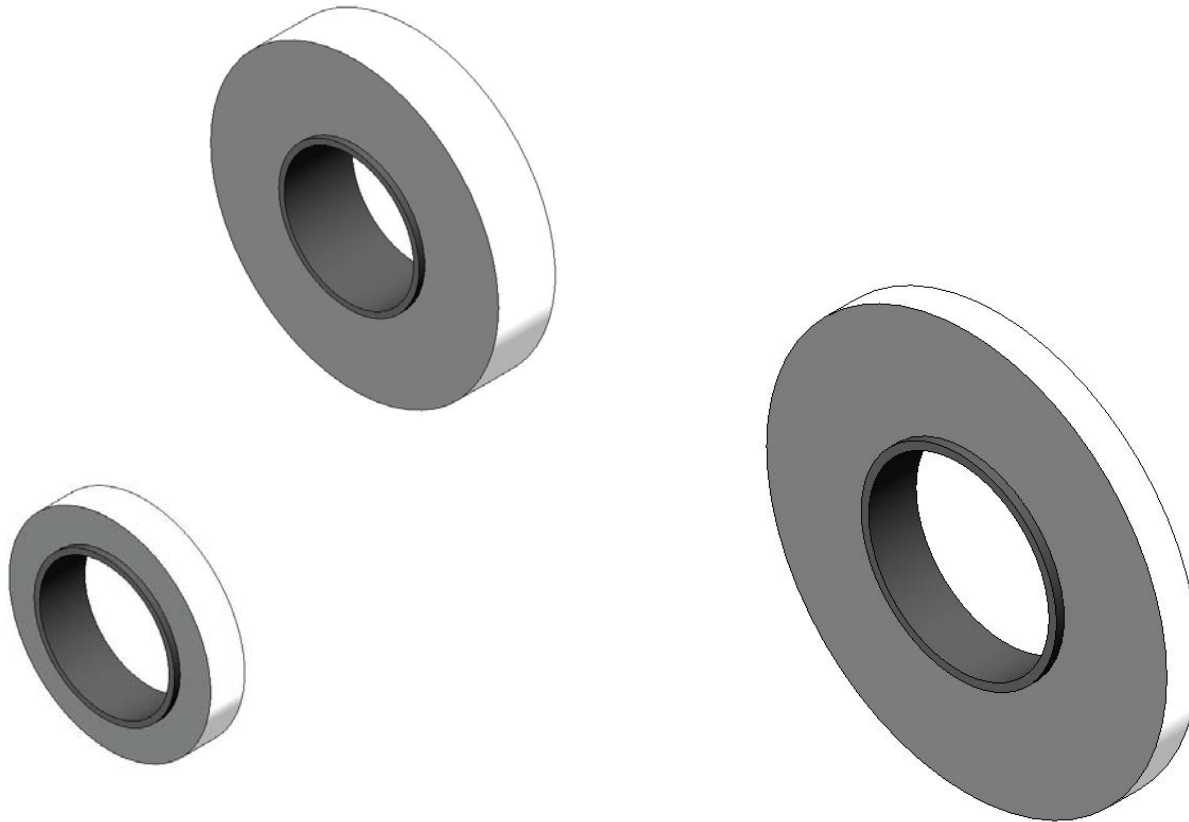
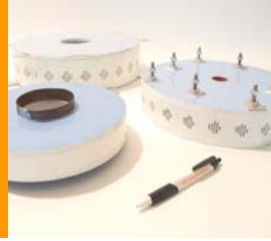
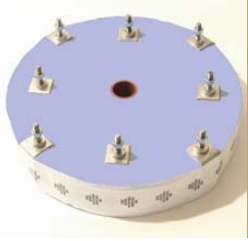
# Consider Making the DC Link Capacitor Round



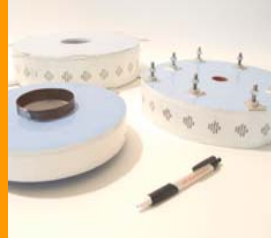
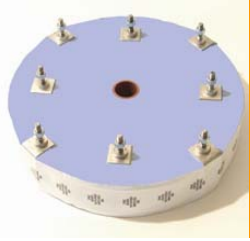
- ⚡ SBE presents a discussion of DC Link Capacitor-related issues, and a solution to the need for a Round Capacitor.
- ⚡ The SBE Power Ring™ Solution:
  - ⚡ Customized Center Hole and Terminal Configuration
  - ⚡ Highest Capacitance Density
  - ⚡ Lowest Possible Losses and Inductance
    - Higher Ripple Current Rating



# Examples of Ring Form Factor Film Capacitors



# Trade-Off Between Capacitance and Center Hole Size

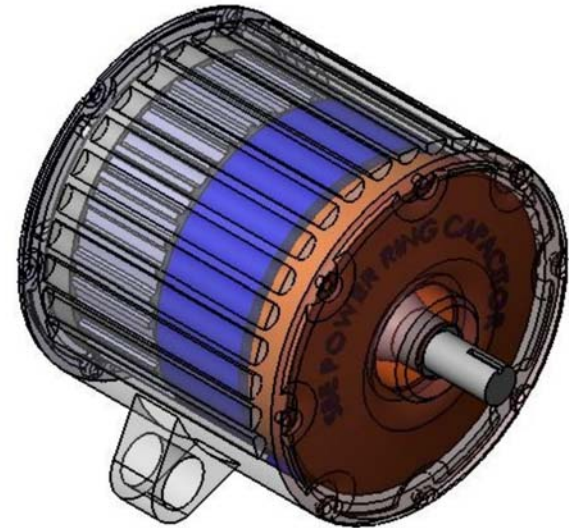


⚡ The presence of the Center Hole:

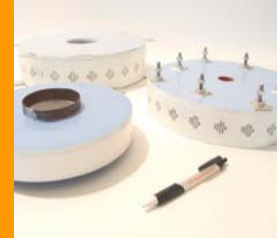
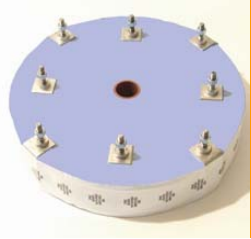
⚡ Can be very useful

⚡ Results in minimal reduction in capacitance

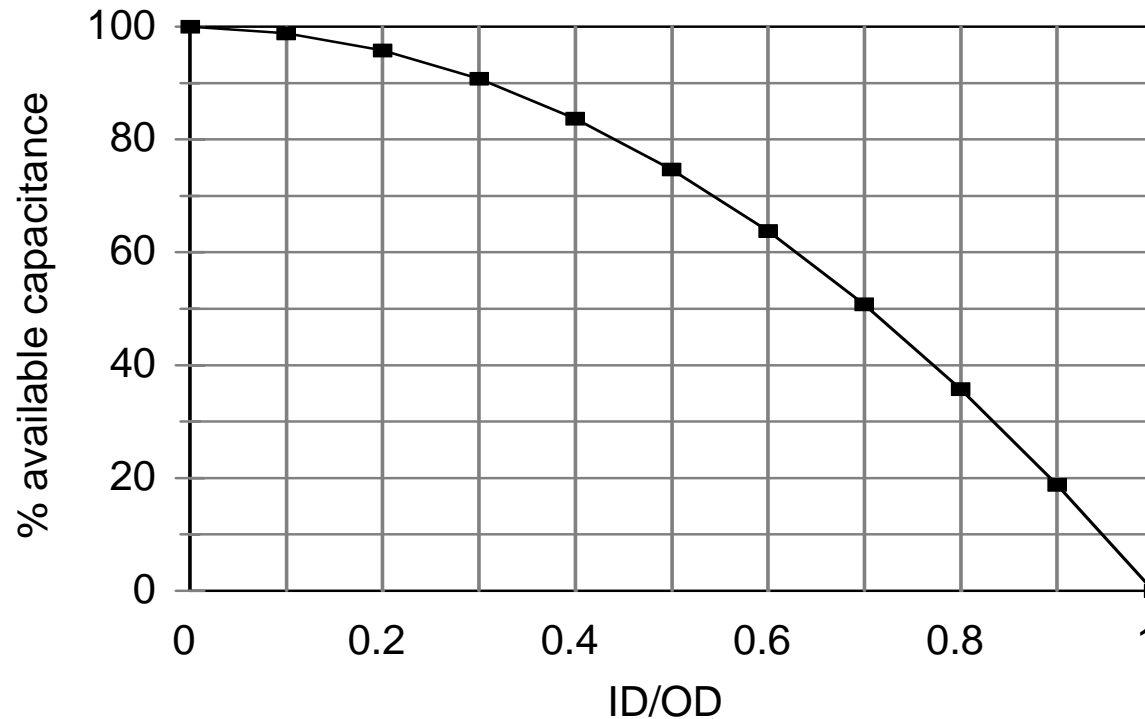
- A 30% diameter hole sacrifices less than 10% of the total available ring capacitance



# Trade-Off Between Capacitance and Center Hole Size



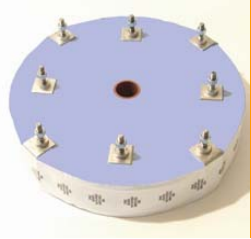
## Capacitance vs. "Hole to OD" ratio



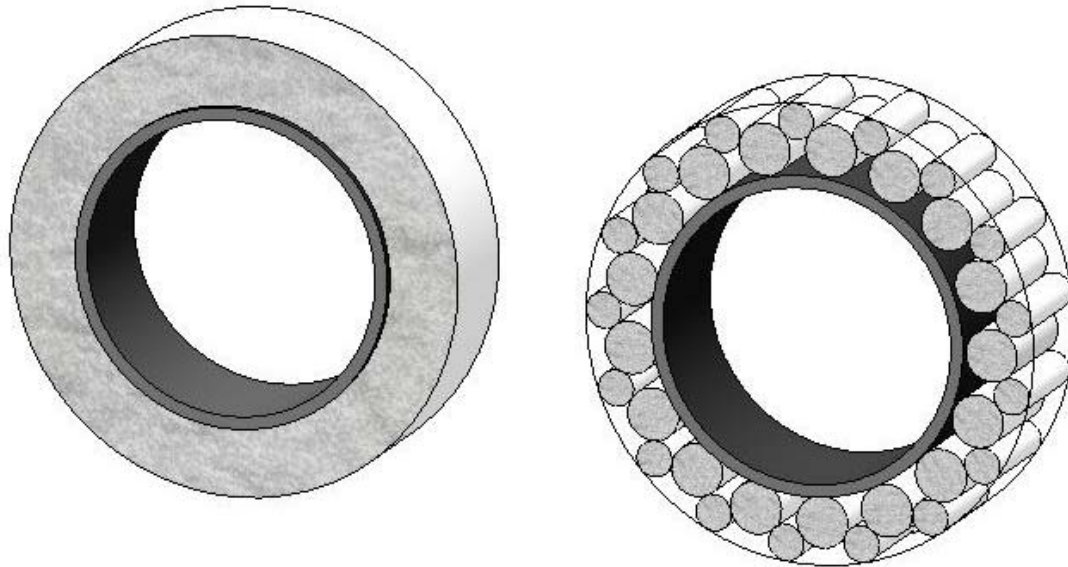
The Hole Subtracts a small percentage of Capacitance



# Other Approaches to a Round DC Link Capacitor Implementation

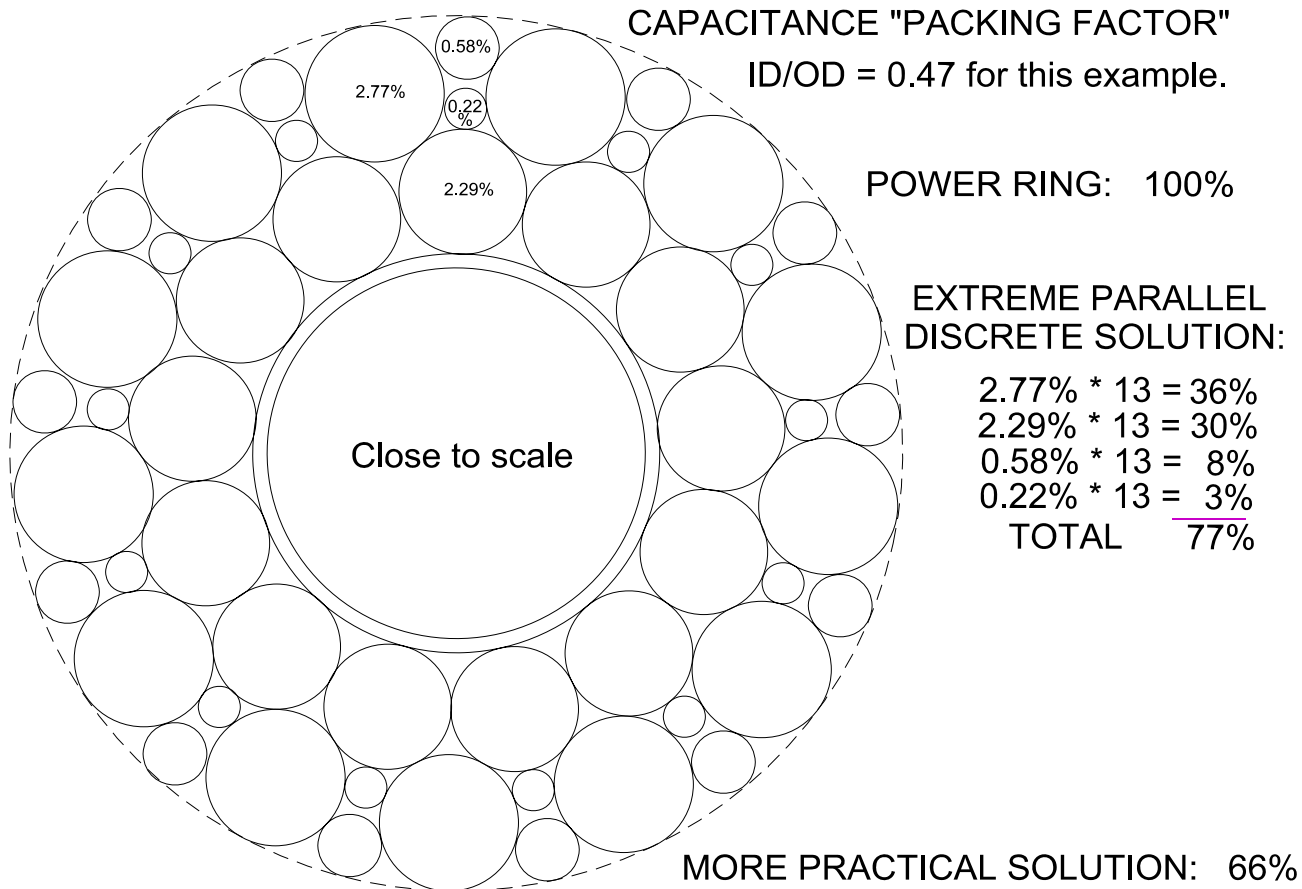
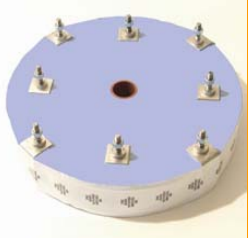


- ⚡ Others have implemented this concept using discrete capacitor windings





# What is the Difference between the Discrete Implementation and the Solid Ring Approach?



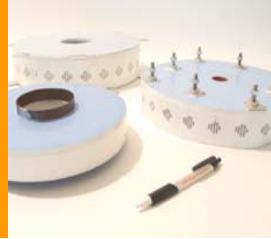
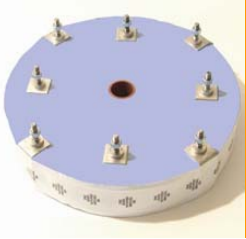
# Available Capacitance of the Power Ring?

⚡ Consider some Capacitor Sizes Relevant to Typical Electric Motors

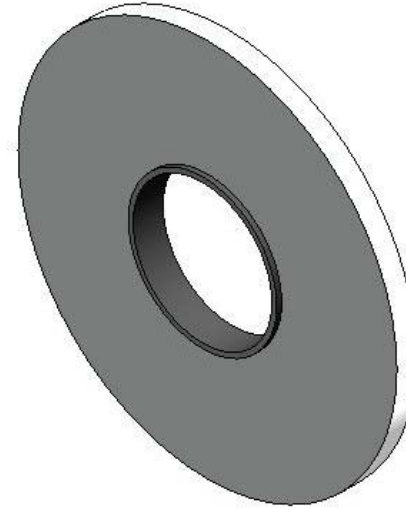
- 4.5 inch ID/7 inch OD
- 4.5 inch ID/10 inch OD
- 5.5 inch ID/15 inch OD



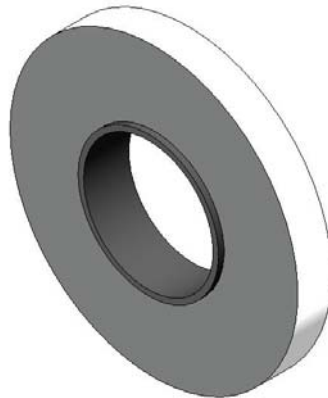
# Available Capacitance of the Power Ring?



4.5 inch ID/7 inch OD



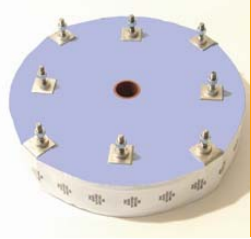
5.5 inch ID/15 inch OD



4.5 inch ID/10 inch OD

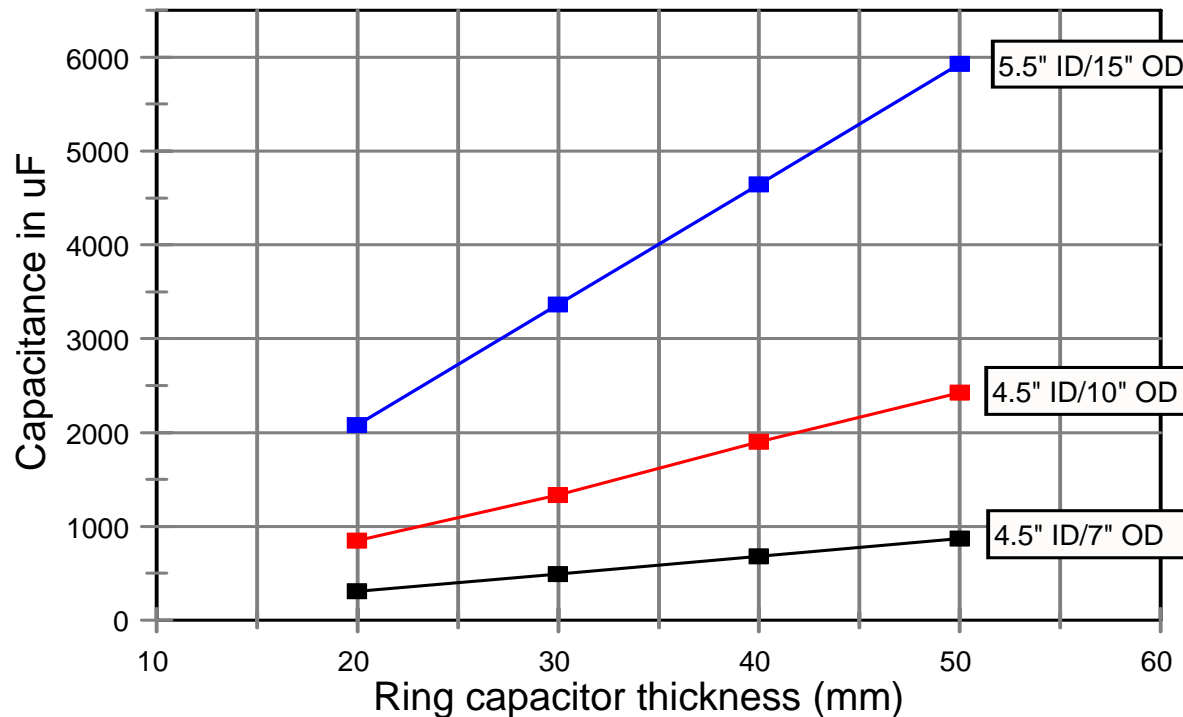


# Available Capacitance of the Power Ring

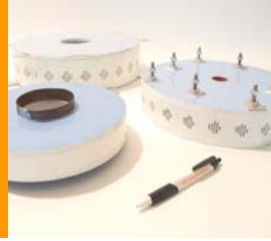
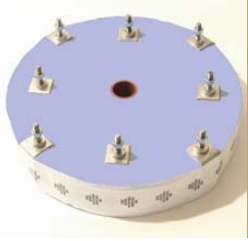


## Available Capacitance

Typical 600VDC design [3.8u MPP film]

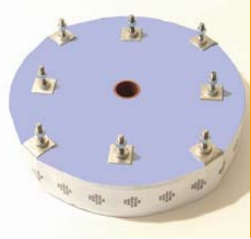


# Available Capacitance of the Power Ring

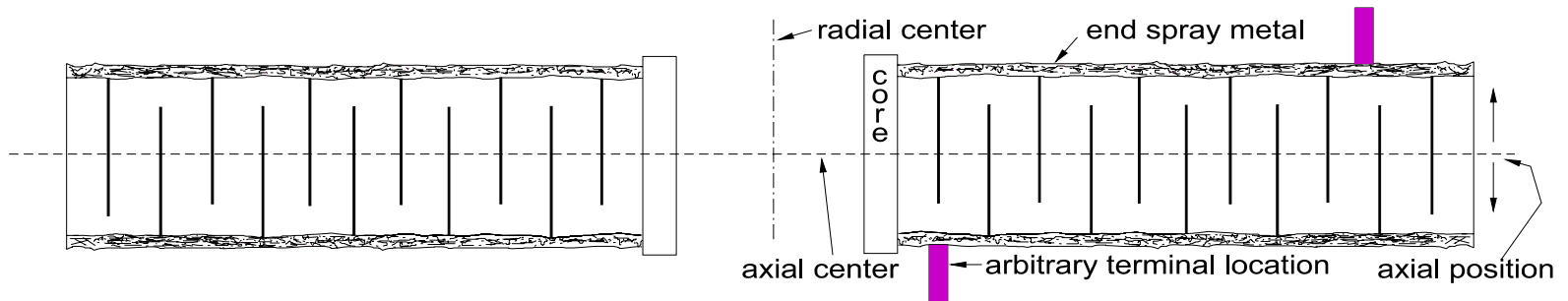
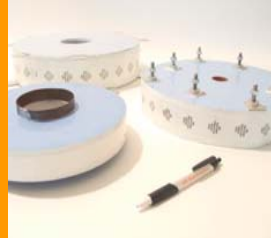


- ⚡ Graph represents a Nominally Aggressive Capacitor Design
- ⚡ Increased Dielectric Stress would allow for more capacitance per volume
- ⚡ But Capacitance change versus thickness will stay the same



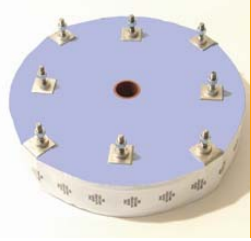


# Ring Capacitor Terms

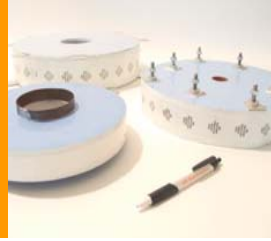


The Large Ring Capacitor behaves as a distributed Circuit Element both Thermally and Electrically

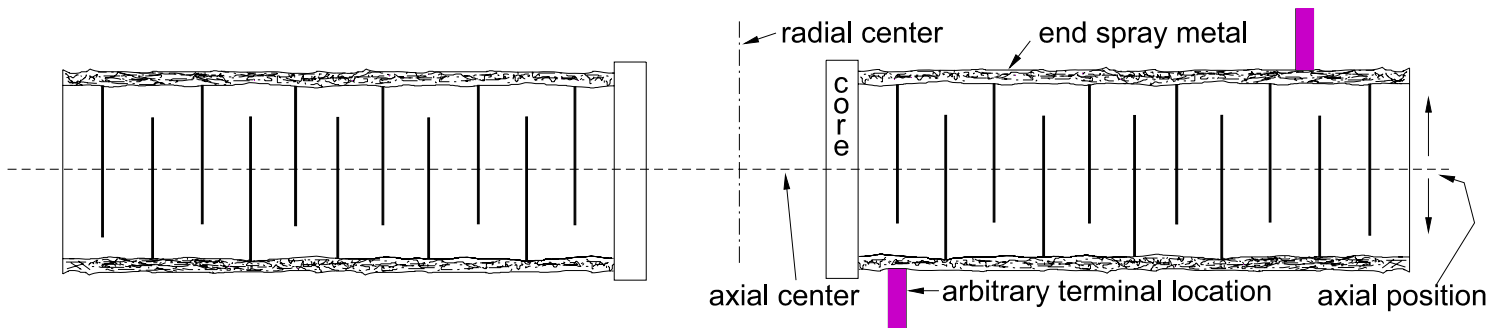


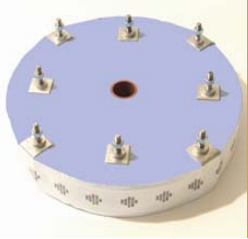


# Effects of Increasing Capacitor Thickness

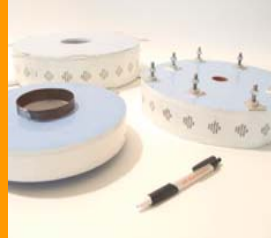


- ⚡ Increased Electrode Contribution to Total Effective Series Resistance (ESR)
- ⚡ Increased Series Inductance
- ⚡ Longer Thermal Path for heat Removal
  - Higher Temperature Rise for a given Dissipation
- ⚡ Capacitor Hot Spot limits overall System Temperature



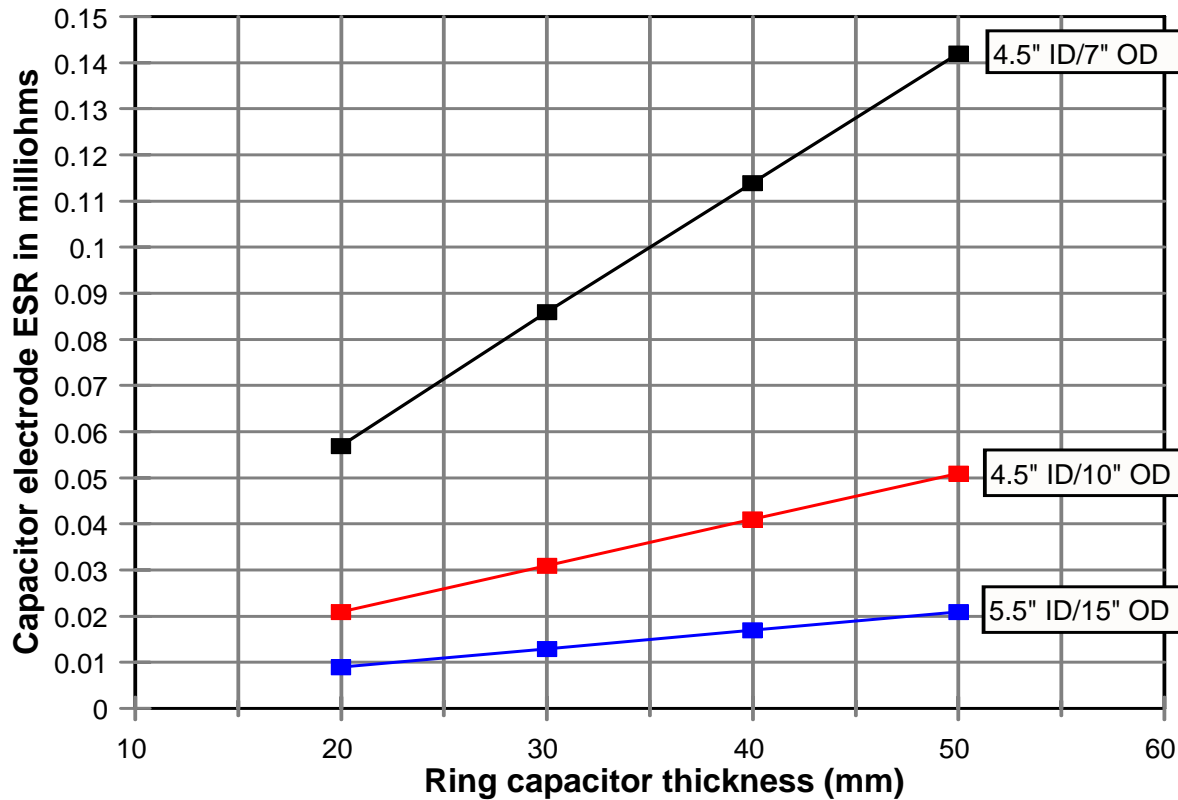


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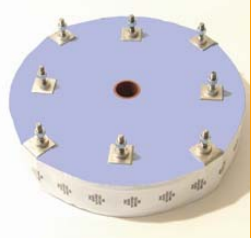


## ESR vs. Capacitor thickness

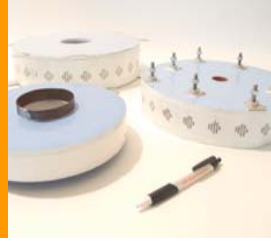
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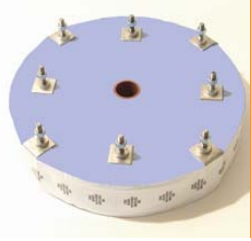


# Trade-Offs for Increased Capacitance

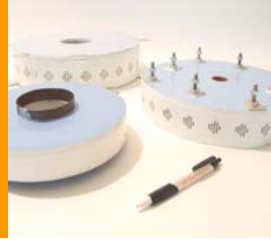


- ⚡ Reducing Film Thickness will also increase ESR and tend to reduce lifetime
- ⚡ Increasing Ring Thickness will result in higher ESR and Thermal Resistance
- ⚡ ESR and Thermal Resistance are prime drivers of Ripple Current Ratings



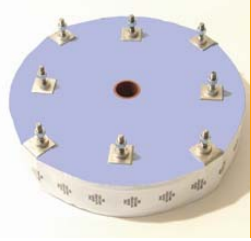


# Ripple Current

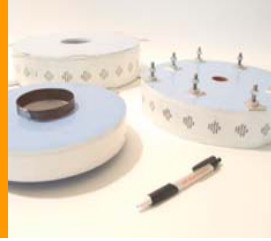


- ⚡ It's a function of Temperature
- ⚡ MPP is usable from  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ , with possible upside (i.e., high crystallinity film)
- ⚡ A “Current Rating” is near meaningless unless the thermal environment is well defined
- ⚡ Traditional Capacitor Current Ratings usually assume “free air convection” (the fine print)
  - An invalid assumption for a Motor Environment



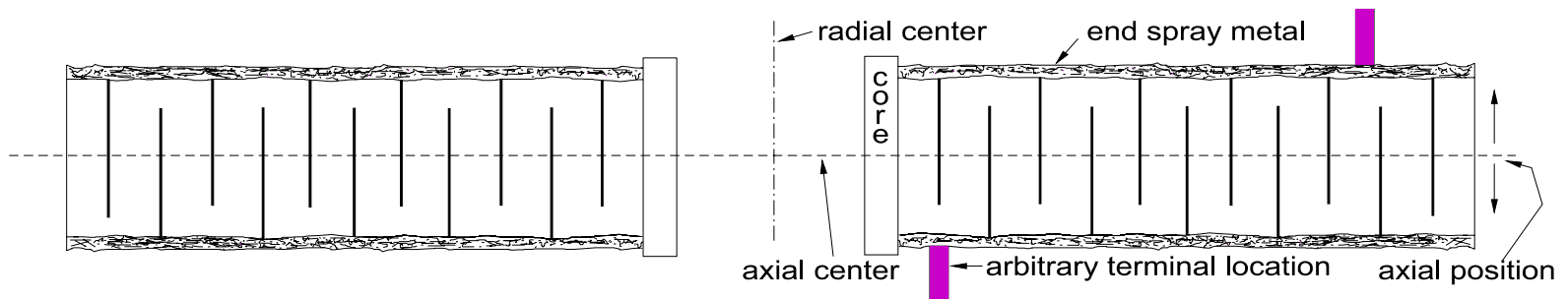


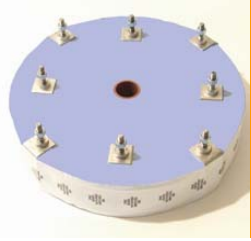
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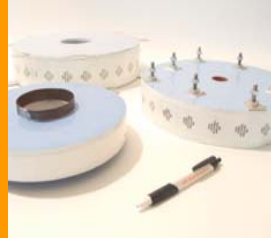
## ⚡ A Thermally Distributed Model Applies

- The Capacitor will see different temperatures at different places
- Thermal Conductivity is not uniform over the capacitor surface



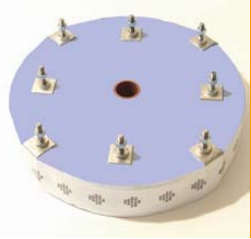


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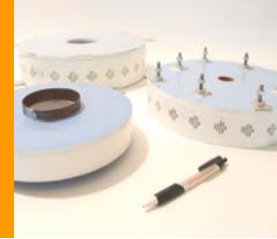


- ⚡ So, as a Capacitor Manufacturer, **how** do we Rate the Ripple Current?
- We need to know the maximum temperature at the End Spray Surface



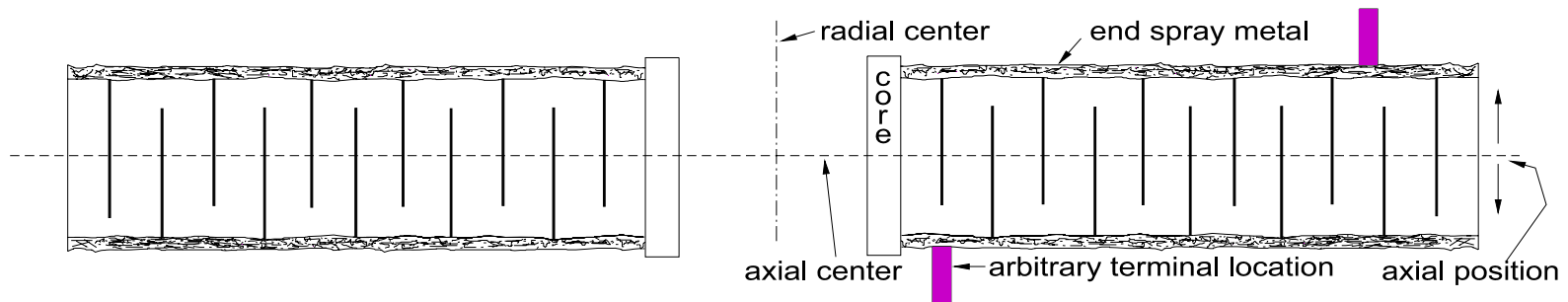


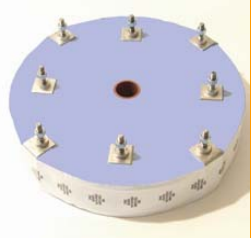
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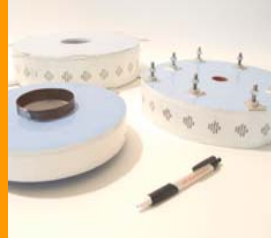
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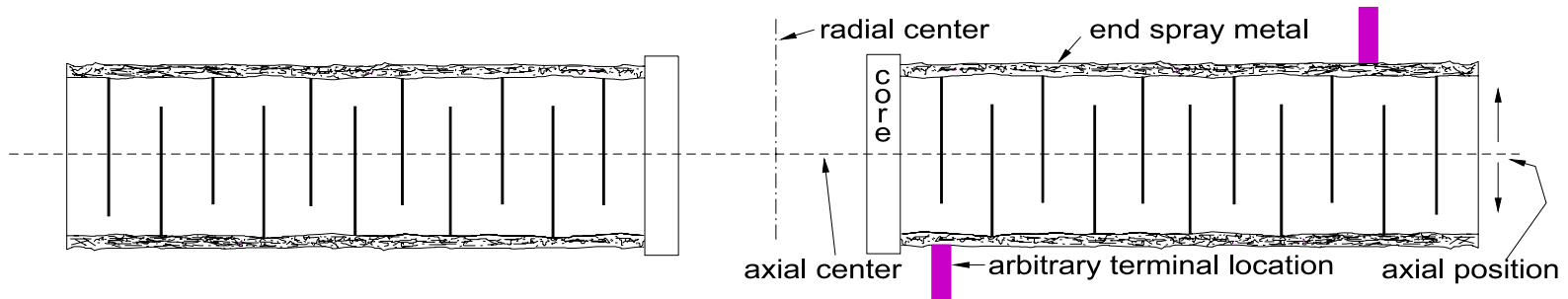




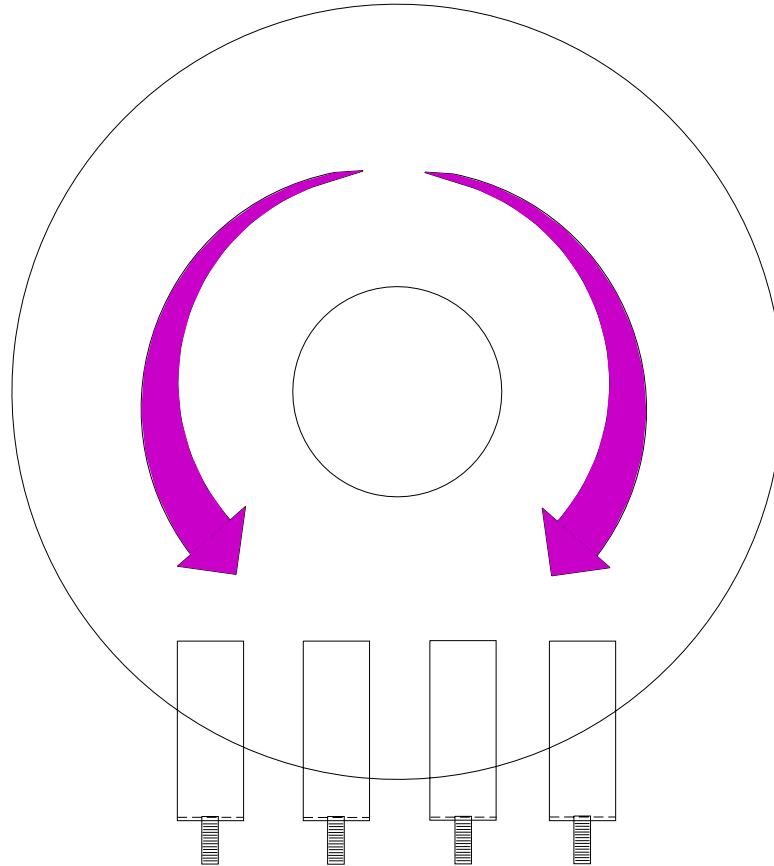
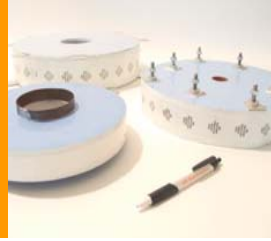
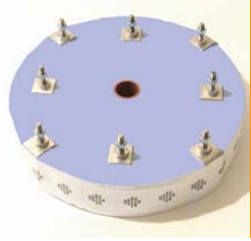
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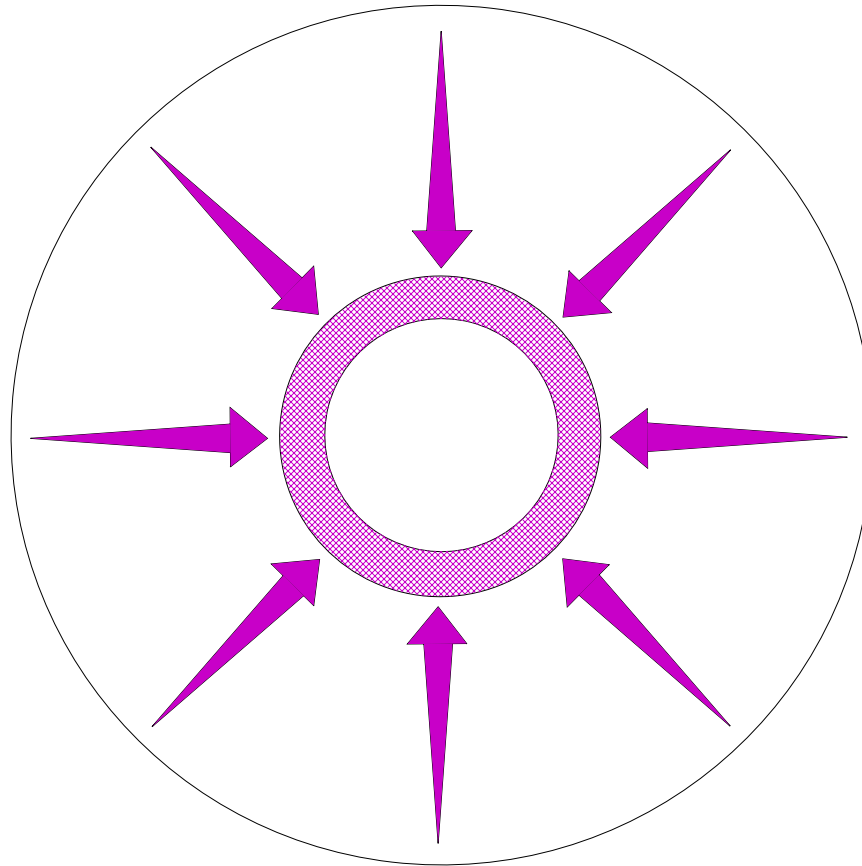
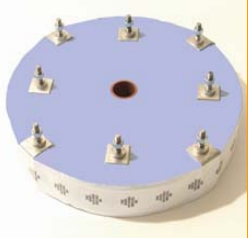
- ⚡ Unlike Conventional Capacitors, the Film Electrode Loss for the Ring Structure is so Low that current in the End Spray can be the dominant Loss Contributor
- ⚡ Capacitor Interface with Bus Structure is Critical to minimize End Spray Losses and therefore will dictate the location of this maximum temperature
- ⚡ Capacitor Hot Spot will be near the terminals



# Ripple Current Rating affected by Terminal Placement

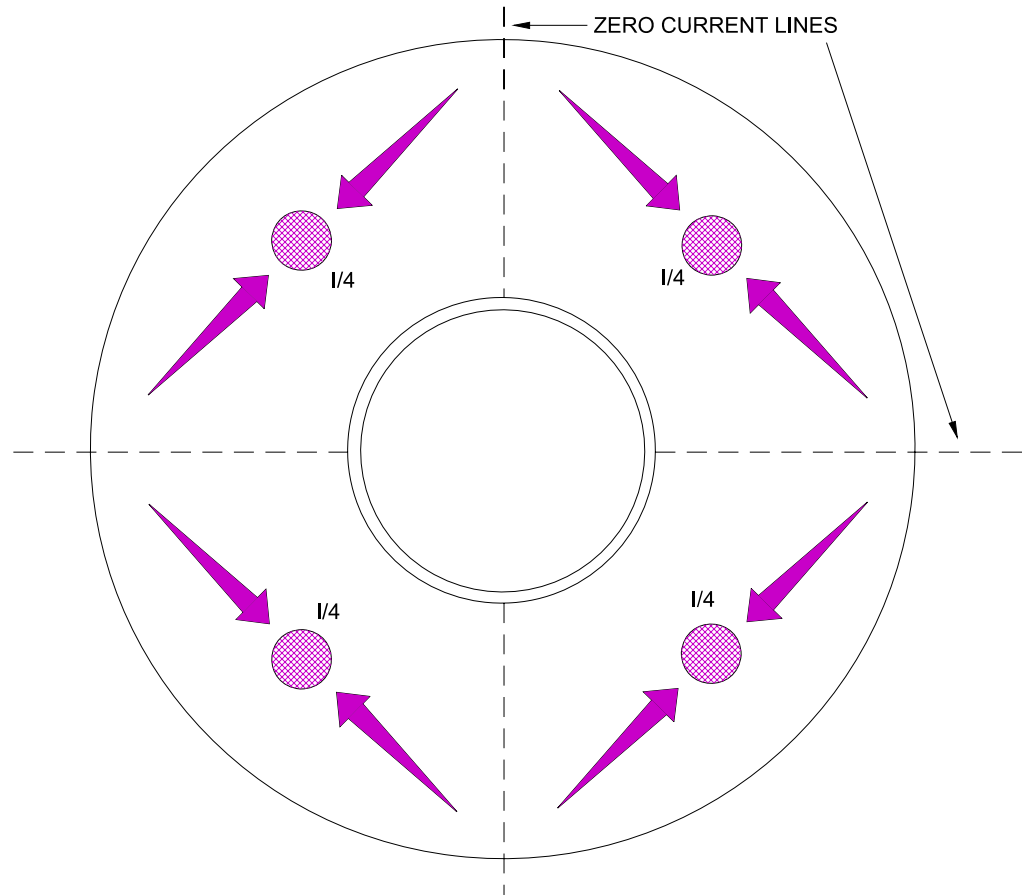
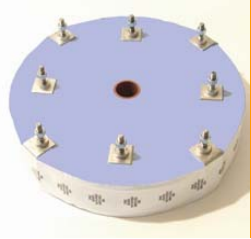


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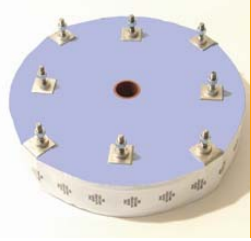


# Ripple Current - Conclusions

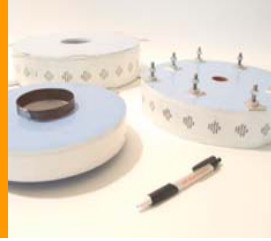


- ⚡ Reducing Current Density in the End Spray results in lower Heat Dissipation and a Higher Ripple Current Rating
  - Multiple Terminals and Optimal Placement Required
- ⚡ Use of a Thin Ring results in a higher Ripple Current Rating
  - Lower Film Electrode Loss
  - Shorter Thermal Path
  - Doubling the Ring Thickness results in halving the Ripple Current Rating
- ⚡ Reducing Capacitor Interconnect Losses will also increase the Ripple Current Rating



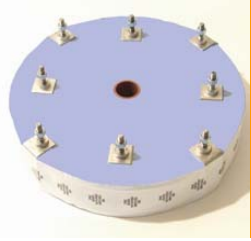


# Capacitor Interconnect Losses

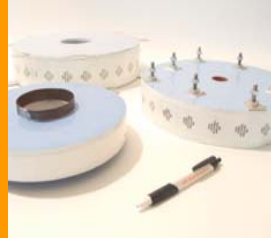


- ⚡ Simulation and Experiments have shown that the Capacitor behaves as a Heat Sink for the Bus Structure Losses!
  - Only considers the AC case
- ⚡ The DC Bus Losses make the above problem even more pronounced
- ⚡ To Truly Optimize Ripple Current Rating, minimize Overall Bus Structure Losses



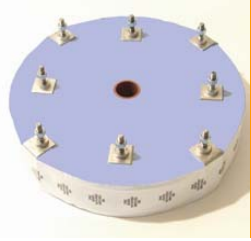


# Bus Structure Losses

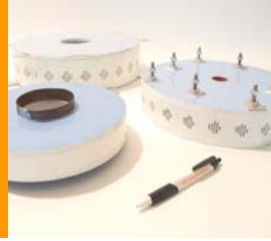


- ⚡ Use the highest voltage that Semiconductor SOA and winding insulation systems will allow
  - Doubling the voltage will reduce bus dissipation by a factor of 4. Will not necessarily change Capacitor size.
- ⚡ Skin Effect Losses can be significant
  - Multiple Connections reduce this effect
  - Be sure to consider the harmonic content of ripple current



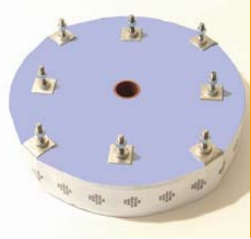


# The Value of Symmetry

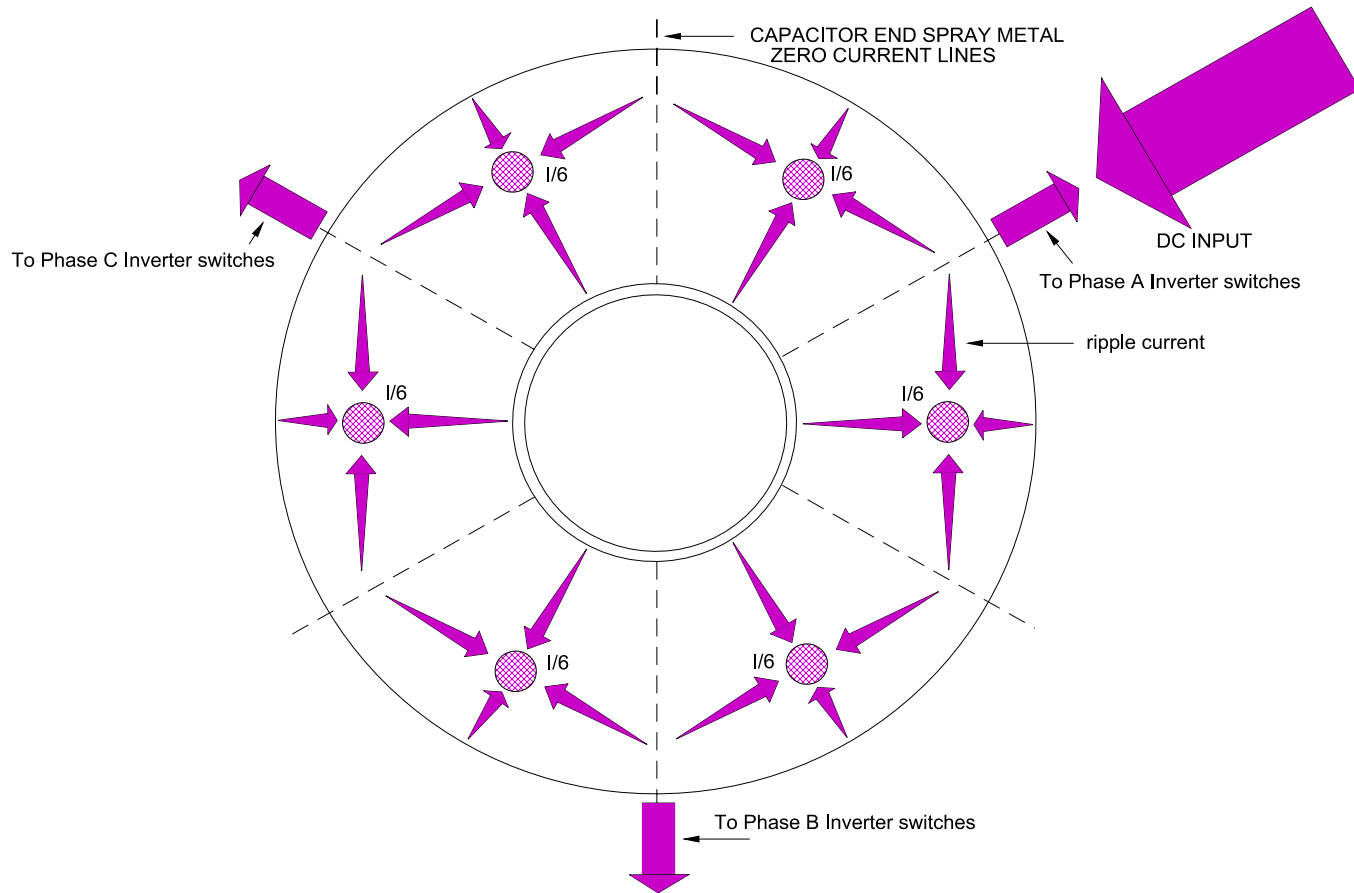
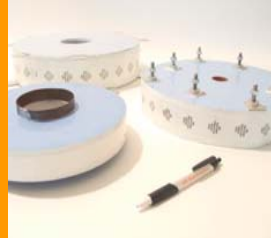


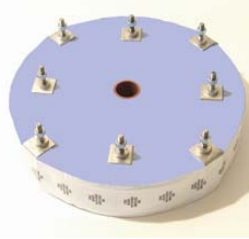
- ⚡ The most efficient performance is optimized by Electrical and Mechanical Symmetry
- ⚡ For 3 Phase Systems, the Inverter power should be withdrawn from the bus at equally spaced locations (120 degrees apart)
- ⚡ If the DC Input is very close to one of the Inverter outputs, the DC losses can be minimized



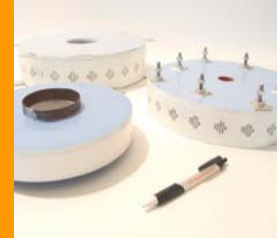


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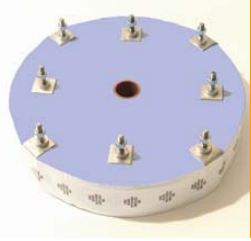


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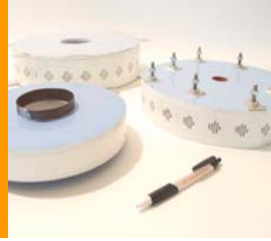


- ⚡ 6 areas on the Capacitor surface with essentially no dissipation (zero current)
- ⚡ 6 terminals divide the ripple current, further reducing dissipation
- ⚡ Remove DC power to inverters between interconnects to more uniformly distribute the ripple current
- ⚡ Apply DC input current very close to the inverter AC outputs to minimize DC losses in the Bus Structure





# Conclusions

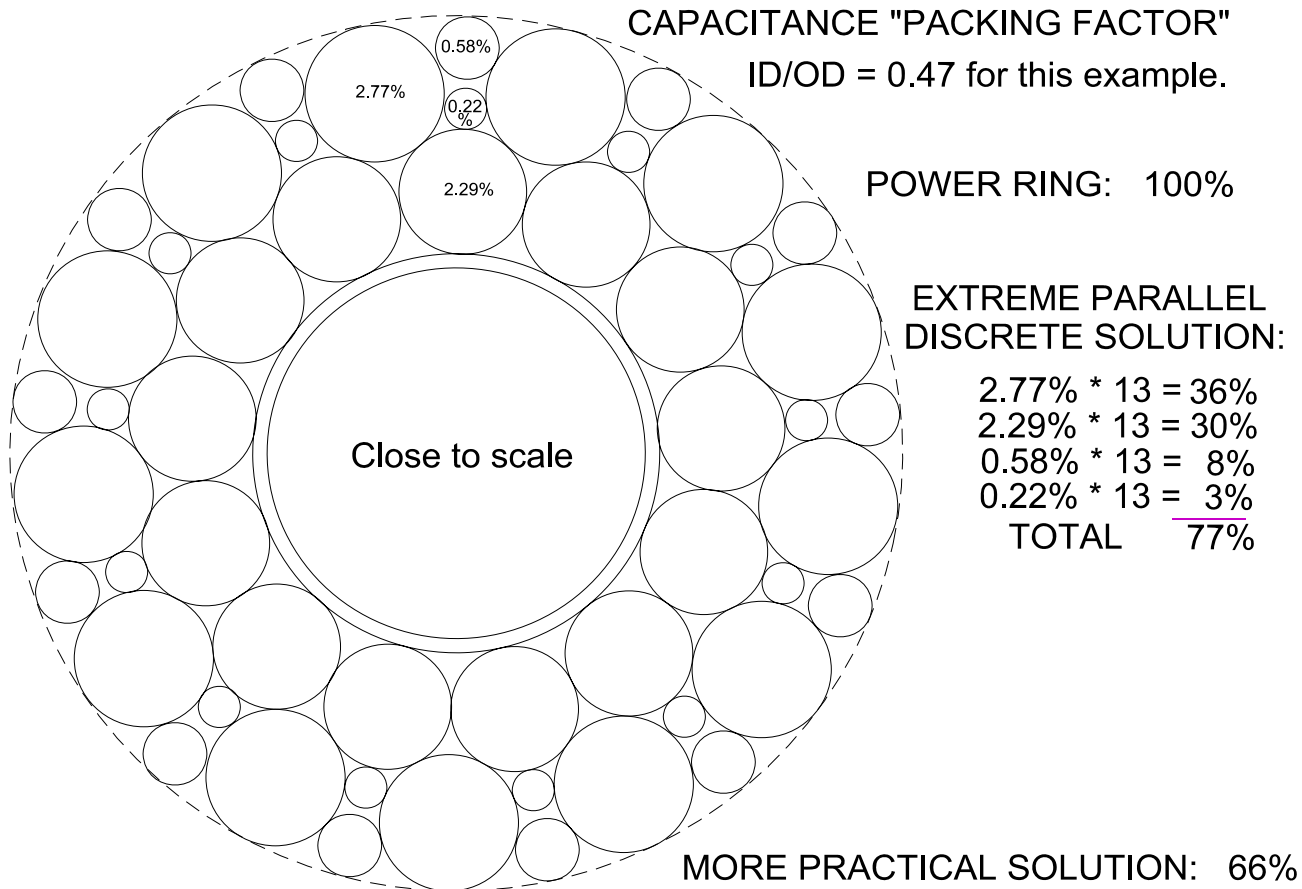
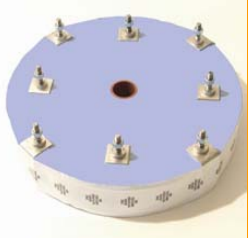


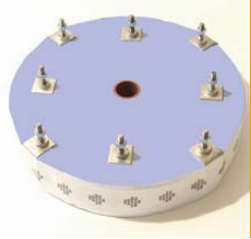
- ⚡ There are great advantages when committed to a round shape of the Capacitor/Inverter
- ⚡ To obtain optimum performance from your E-Drive System, close interaction with the Capacitor Manufacturer is required
- ⚡ The advantages of the Power Ring over a discrete implementation are significant in both space and allowable ripple current
  - Ripple current has to be reduced by the “Packing Factor” percentage



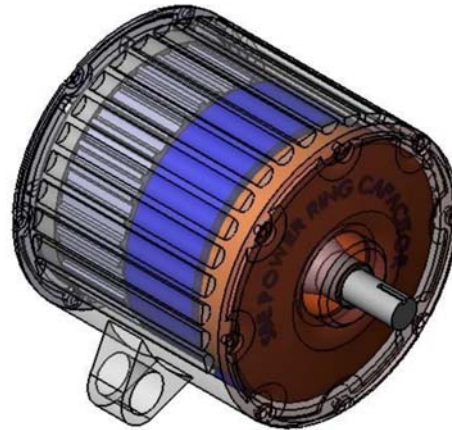
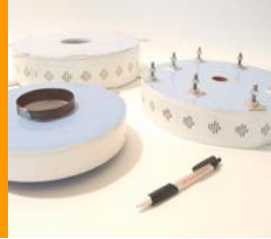


# What is the Difference between the Discrete Implementation and the Solid Ring Approach?





# SBE, Inc.



**Thank you!**  
**Come see us at Booth 23**

