Optimized DC Link for Next Generation Power Modules

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Abstract

The market leaders in IGBT technology are now introducing next generation "six-pack" modules to enable increased power density and reduced cost for automotive traction drive applications. However, the potential gains offered by these modules can only be harvested using an optimized DC link with integrated capacitor/bus topology. Two integrated capacitor/bus solutions have been designed to support the new Infineon HybridPACK™ Drive module with the lowest possible µF/kW ratio and minimized equivalent series inductance. Simulation and design results are presented along with third party testing data for a complete inverter.

1. Introduction

- Next generation power modules are targeting increased power density and efficiency.
- An optimized DC link cap/bus is needed to fully exploit such modules
  - Maximize Ampere per micro-Farad rating
  - Minimize ESL and voltage overshoot for maximum working voltage
- Integrated cap/bus is the answer as previously demonstrated for wind power where smaller µF/kW ratio facilitated fitting a 1MW inverter into a 500kW frame [2].
- Apply the same approach to develop optimized DC link for Infineon HybridPACK™ Drive (HP Drive FS820R08A6P2xx) [1]
  - Horizontal configuration
  - Vertical configuration
  - Third party test data presented for horizontal configuration

2. DC Link Requirements

- Requirements for HP Drive DC link capacitor are maximum needs of the Infineon HP Drive at full power cycle
  - 450V < V_{dc} < 550V
  - 75Arms < I_{ripple} < 125Arms continuous
  - 50°C < $T_{coolant}$ < 85°C
  - 500µF
  - 10,000 hours min under full drive cycle conditions

3. Horizontal Layout Design

- The horizontal configuration is presented in Figure 1.
  - Two 250µF annular film capacitor windings are directly integrated to a laminated bus structure
  - DC terminals located opposite IGBT inputs to minimize "current hogging"
  - Shortest possible connection length combined with "through hole" connections to module gives the lowest possible inductance
- Thermal profile subject to 50Arms ripple with an 85°C boundary defined on the capacitor case is presented in Figure 2.

Figure 1: Integrated capacitor/bus DC link from SBE Inc.

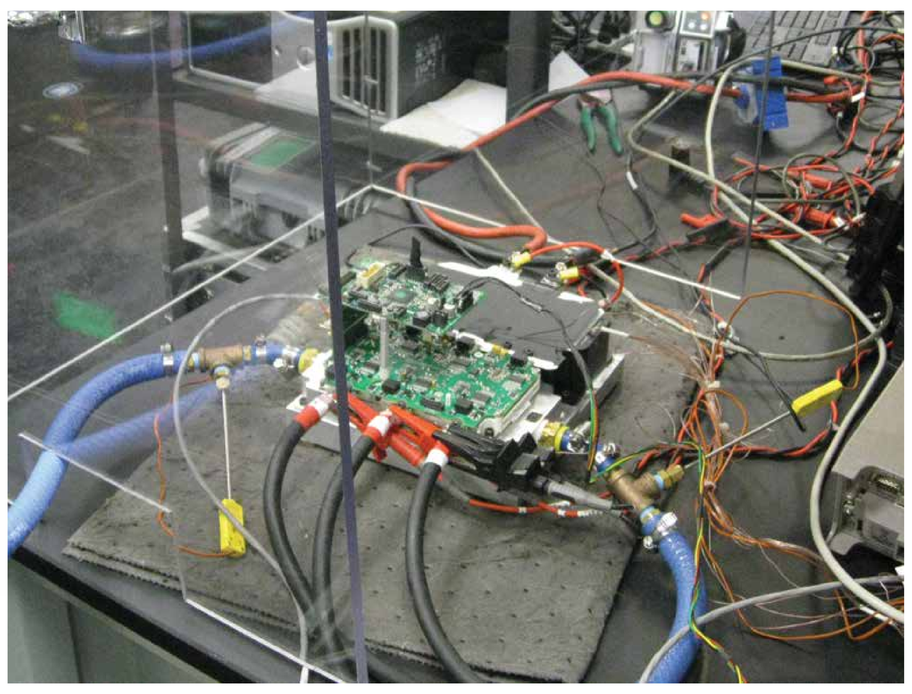


Figure 4: Complete inverter test setup used at the National Transportation Center at Oak Ridge National Laboratory

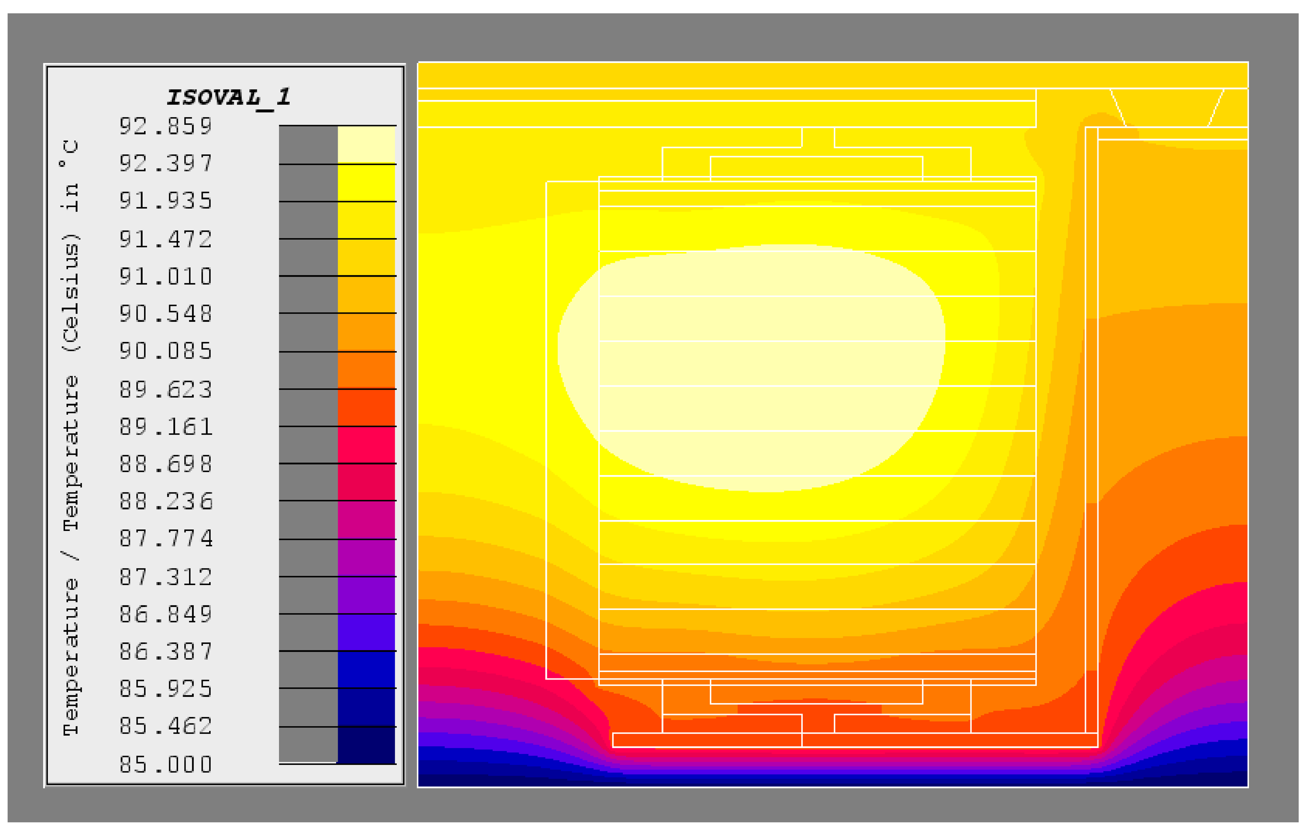
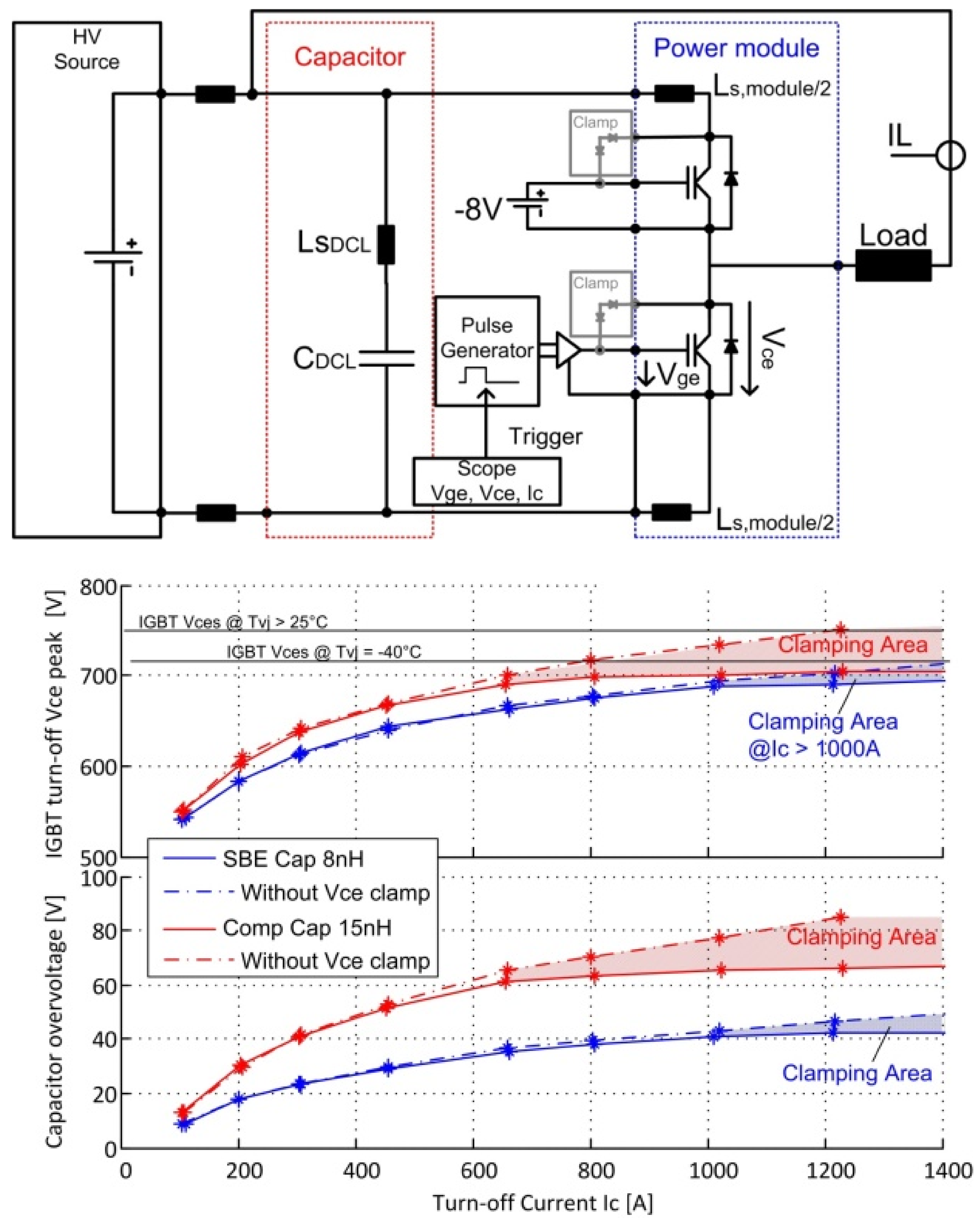


Figure 2: Thermal profiles for single capacitor winding in the assembly



(a)

(b)

Figure 3: Overshoot testing DC link capacitors at Infineon
(a) test circuit, (b) turn-off overvoltage at 500Vdc working voltage

4. Inductance Measurements

- Ring-out testing performed at SBE using previously described method [4]
  - ESL is 8.4nH
- Independent measurements performed by Infineon
  - ESL is about 8nH
- Practical considerations
  - Vce must be limited to less than the Vces -40°C specification of the IGBT/diode chipset
  - Active collector gate clamping is implemented to limit Vce to <710V for the HP Drive
    - ◇ Repetitive clamping circuit activation must be avoided to prevent damaging the TVS diodes which can lead to module failure
  - Higher gate drive resistance can be used with penalty of lower performance
  - Best utilization of working voltage is achieved by minimizing stray inductance
- Comparison of IGBT turn-off using circuit of Figure 3a is presented in Figure 3b for at 500V working voltage
  - 8nH SBE horizontal cap/bus: Low overvoltage, useable transient current range up to 1000A at 500V and full switching speed
  - 15nH conventional capacitor: Clamping circuit activates above 500A at 500V and switching speed must be reduced for safe operation
- A low inductance DC link cap/bus is mandatory for applications that require high working voltage and full switching speed to achieve the lowest possible inverter power loss
- Higher stray inductances provide a larger overvoltage at turn-off which thus limits the maximum useable working voltage.

5. Inverter Testing Setup

- Infineon Hybrid Pack Drive with cooling plate, gate driver, and micro-controller was combined with SBE 700A186 cap/bus test kit
- Inverter testing performed at Oak Ridge National Laboratory National Transportation Research Center per Figure 4
  - Static load connected in floating Wye
  - Yokogawa WT1800™ power analyzer to measure efficiency
  - Embedded thermocouples on cap/bus assembly
  - Coolant temperature of 22°C and a flow rate of 6.4 lpm
  - The inverter power was 35kW continuous

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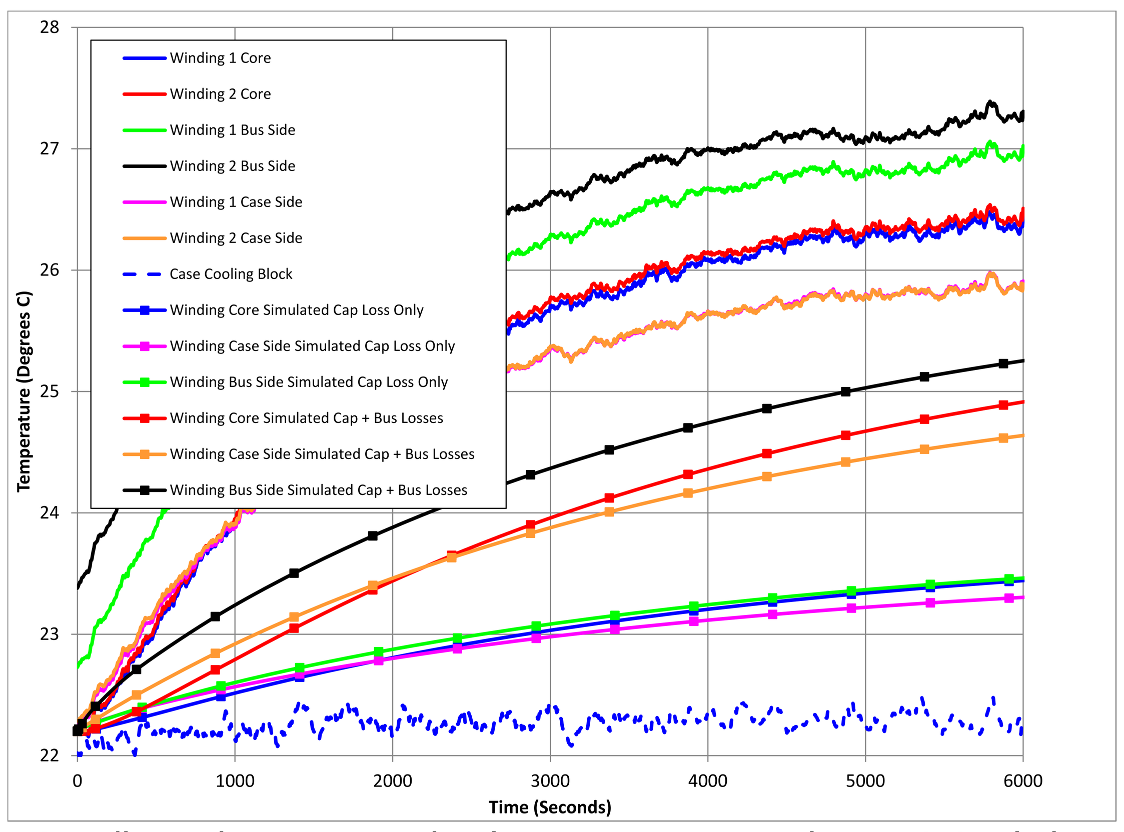

Figure 5: Capacitor/bus thermocouple data as compared to original design simulation: Top six curves represent measured data, bottom curves show simulation with capacitor losses only, middle curves show simulation with capacitor and bus losses

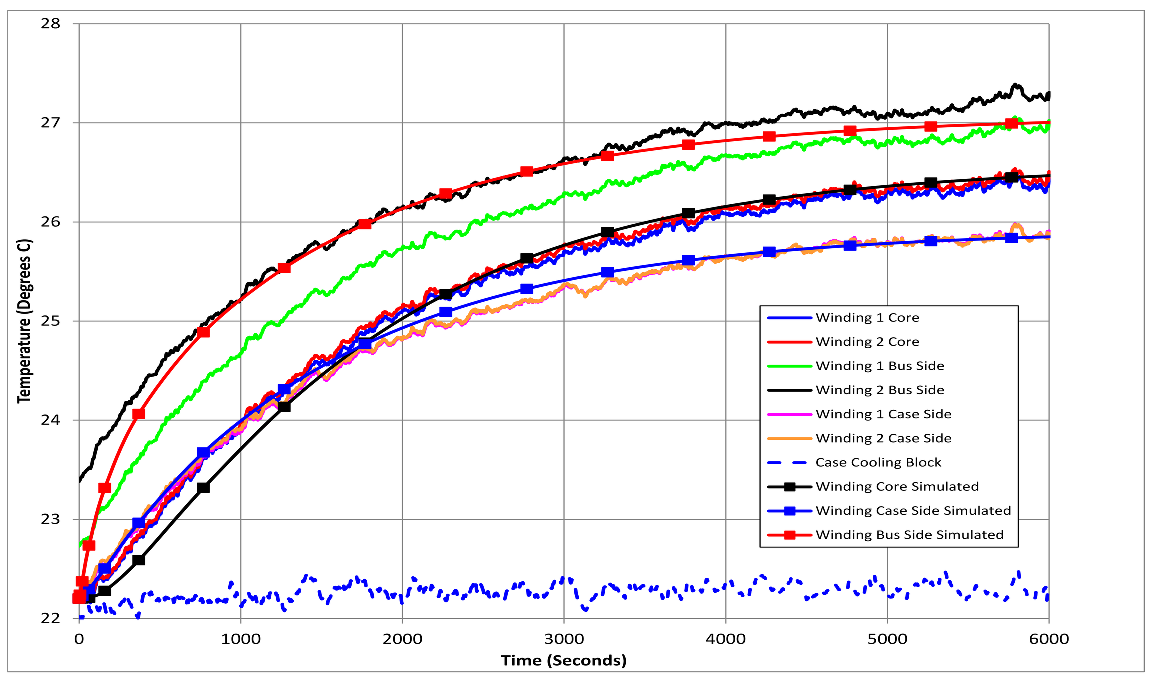

Figure 6: Improved simulation accounting for additional thermal path and addition of IGBT losses to fit test data

6. Inverter Testing Results

- Power analyzer output
  - 35kW, 400Vdc, 8kHz
  - New automotive EDT2 IGBT chip for HP Drive strongly outperforms last IGBT generations
- While test power is well below capabilities of HP Drive and cap/bus some very useful data was obtained
  - Compare thermocouple data to simulation results per Figure 5
    - ◇ Hotspot temperature is too low
    - ◇ Thermal time constant is too slow
  - This indicates two things
    - ◇ Some fraction of IGBT chip and terminal losses are coupled to bus from power module tabs
    - ◇ There is an additional path from bus to ambient
  - Hotspot temperature can be deconstructed into a simple model
    - ◇ $\Delta T = P_{cap} \times R_{Tcap} + (P_{bus} + P_1) \times R_{Tbus}$
    - ◇ P_1 is fraction of chip and terminal losses flowing to bus from IGBT tabs
  - Adjust simulation to fit
    - ◇ Parallel thermal resistance of 2.45°C/W from the bus to 22°C ambient
    - ◇ 1.96W of power is supplied to each winding from the bus
    - ◇ Good match to measurements per Figure 6
  - Relative contributions to temperature rise of cap
    - ◇ 4.8°C = 0.27W x 1.95°C/W + (0.34W + 1.96W) x 1.8°C/W
- Now consider effect of doubling power to 70kW and raising coolant to 85°C
  - Double current: Cap and bus losses increase by 4x
  - Double current: IGBT chip and terminal losses increase by factor of 2.5
  - Increase temperature: Cap bus losses scale by thermal coefficient of resistance
  - Increase temperature: IGBT chip and terminal loss contribution increases by about 6%
  - Capacitor hotspot temperature is shown in Figure 7
  - Use data to generate rating curve on the basis of cap/bus losses per Figure 8
- Based on previously presented life test data [5] a life of 10,000 hours can be achieved with a hotspot temperature of 100°C operating at 400Vdc
  - 10,000 hour life at 70kW with 84°C coolant

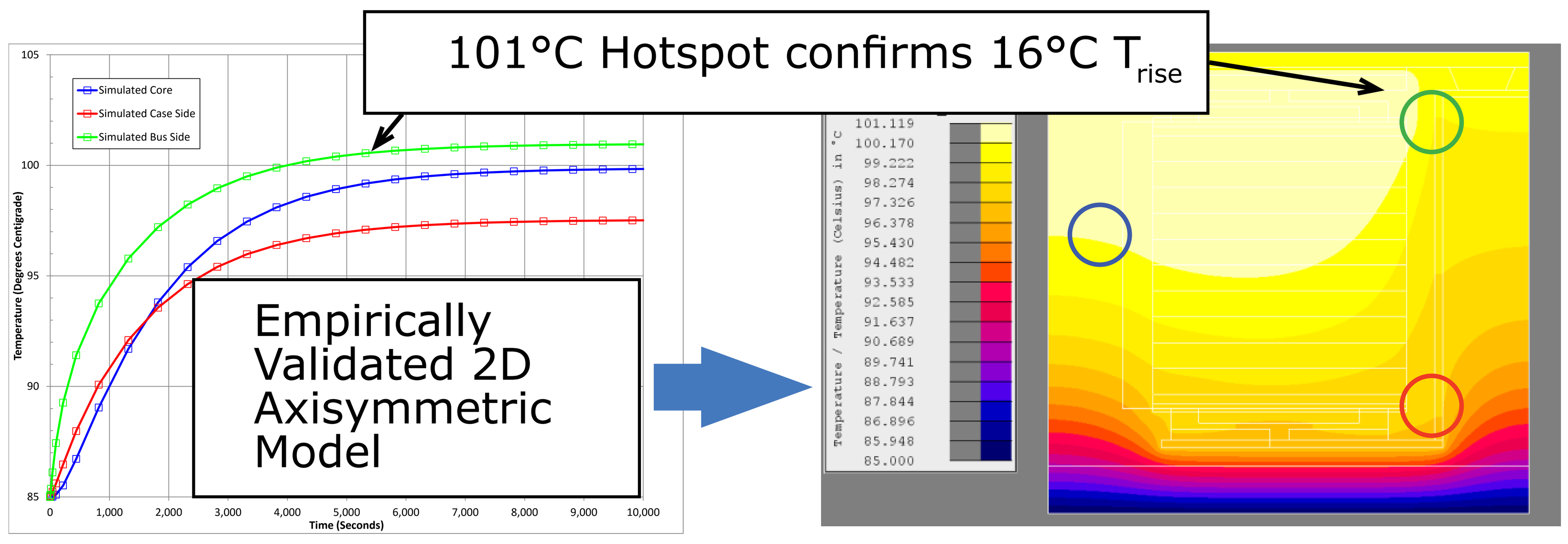

Figure 7: Capacitor temperatures after scaling inverter test results from 35kW to 70kW

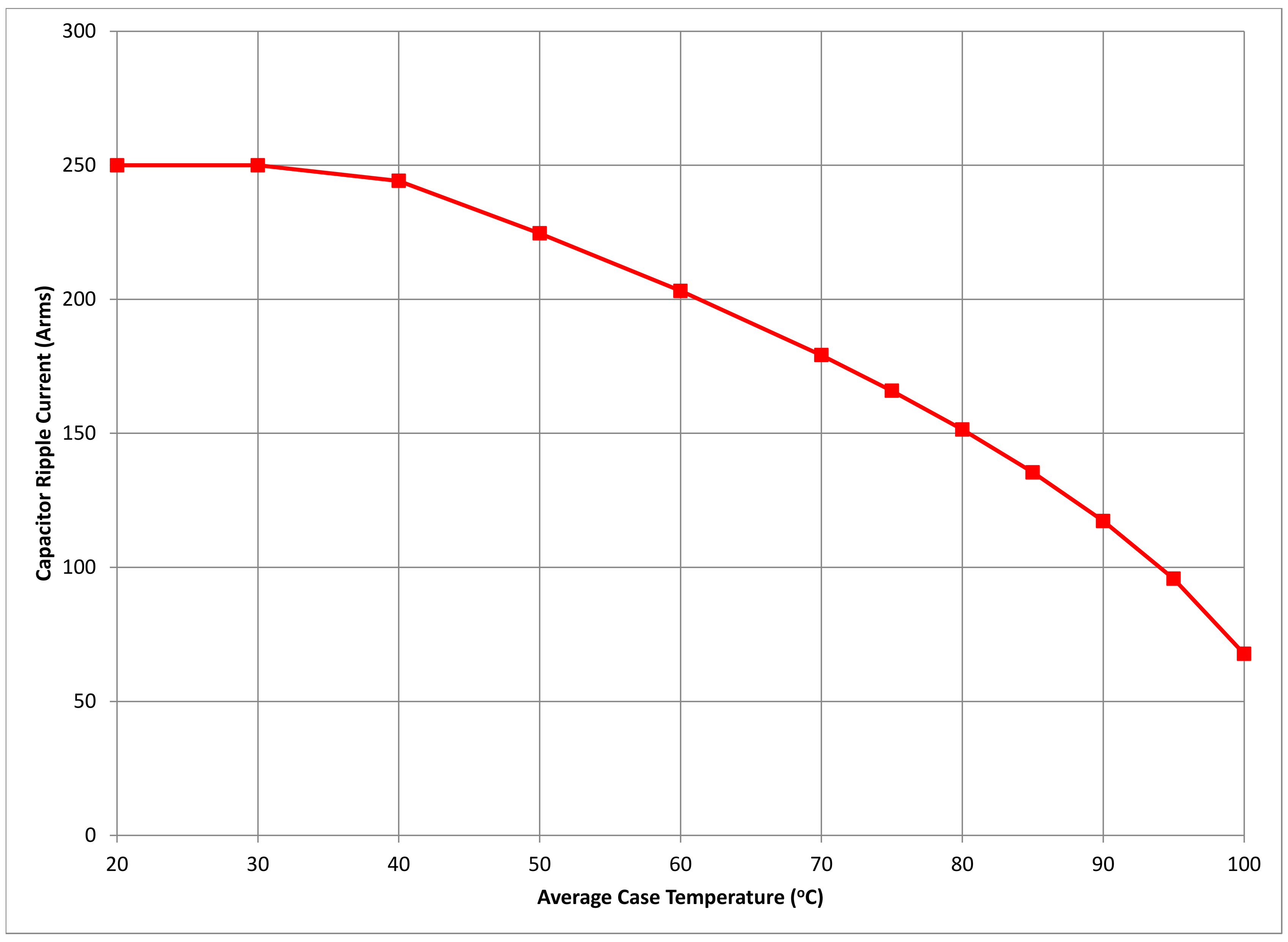

Figure 8: Continuous current rating for the SBE 700A186 horizontal test kit based on inverter test data with capacitor and bus losses only

- Using the same scaling assumptions, consider 100kW at 400Vdc
  - 10,000 hour life at 100kW with 70°C coolant
- HP Drive is intended for 50-150kW (peak) applications and SBE 700A186 is fully capable of supporting the top end of this range for high performance EV
  - 150kW peak can be safely managed for short durations as part of realistic drive cycle

7. Conclusion

- Horizontal and vertical configuration DC link cap/bus test kits designed for Infineon HybridPACK™ Drive power module [1]
  - Horizontal kit has 50% lower ESL than conventional DC link cap
    - ◇ Minimize overshoot and enable higher working voltages and faster switching speeds for best efficiency
  - Vertical kit supports higher performance due to bus cooling with small ESL penalty
  - Third party testing at ORNL NTRC has provided critical data for horizontal kit
    - ◇ Scaling results to practical conditions
      - ▪ SBE 700A186 cap/bus supports 100kW continuous operation at 70°C coolant and 400Vdc with 10,000 hour life
      - ▪ SBE 700A186 (500V and 500µF) therefore supports full utilization of the Infineon HP Drive

References

Included in full paper

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