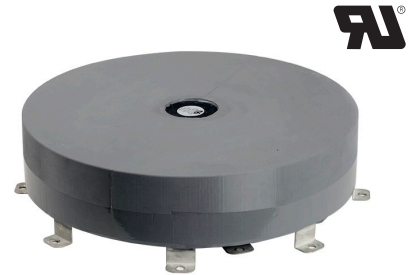


Power Ring Film Capacitor™ 500 µF, 700 Vdc

The 777D50797-109 Power Ring is a UL Recognized 700Vdc, 500 µF DC Link Capacitor with an ESR of 400 micro-Ohms at 20kHz and an ESL of less than 5nH.



Electrical Specifications

SBE Part #: 777D50797-109

Capacitance/Tolerance: 500 µF ±10%

DC Voltage Rating: 700 Vdc

Dielectric/Construction: Metallized polypropylene.
Single section design

Dielectric Withstand: Units 100% tested at DC potential of 950 Volts for two minutes at 25°C

UL Recognition: UL810

UL File #: E364956

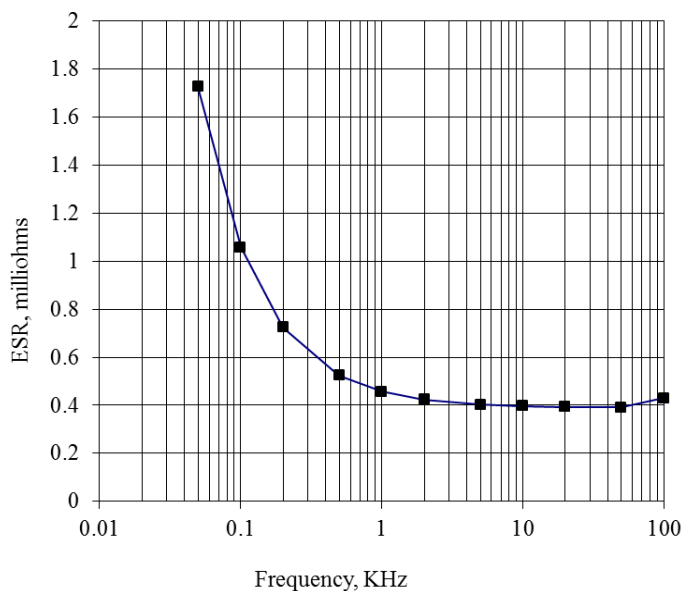
ESL: Less than 5 nH in a suitable laminar bus structure

Operating Temperature: -40°C to +85°C at full DC voltage rating

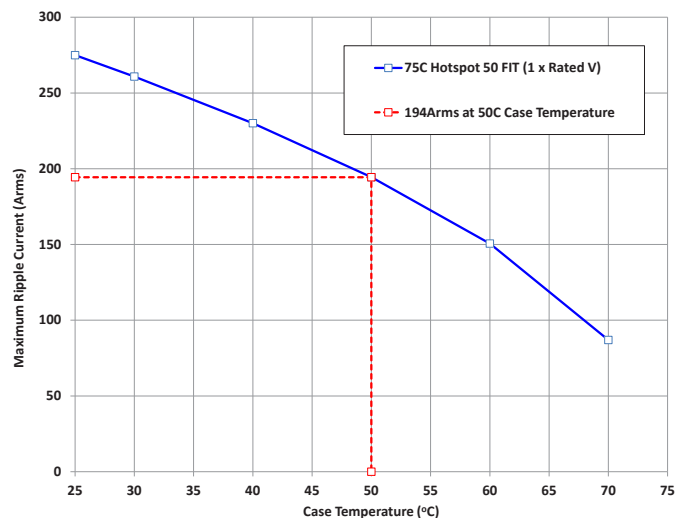
Voltage, Temperature De-rating: Contact SBE for applications above 85°C

System Fault Current Rating (external to the capacitor): 10,000 Amps maximum

Typical ESR vs. Frequency:



RMS Current Rating:



SBE reserves the right to amend design data

Thermal Specifications

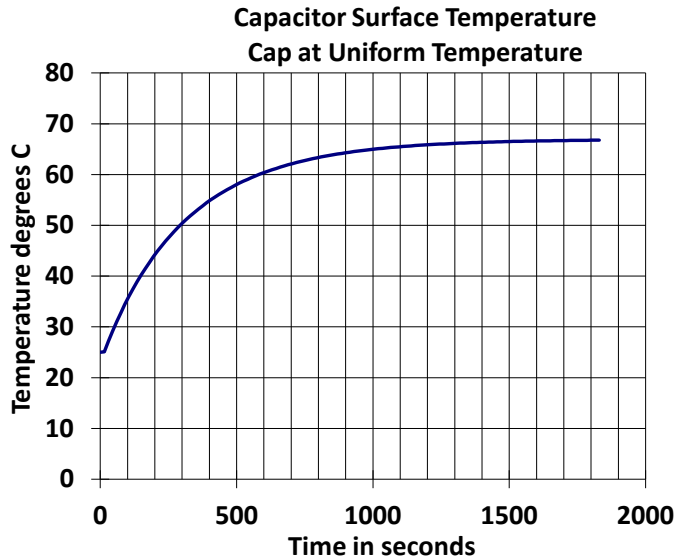
Here are two representations of “Capacitor Surface Temperature over Time” for two specific Thermal Resistances of 1°C/W and 0.5°C/W.

Notes regarding these graphs:

- The thermal resistance is that from capacitor to application. This is a function of the application environment, not the capacitor itself.
- The capacitor can handle extreme current for small duty ratios. Trise occurs very slowly. This is because the capacitor has a high specific heat.
- These charts can be adapted for other currents by multiplying y axis values for any time by $(I_{app}/100)^2$
- Internal capacitor Trise is added to the capacitor surface/terminal temperature.
- Terminals are assumed to be at case temperature.

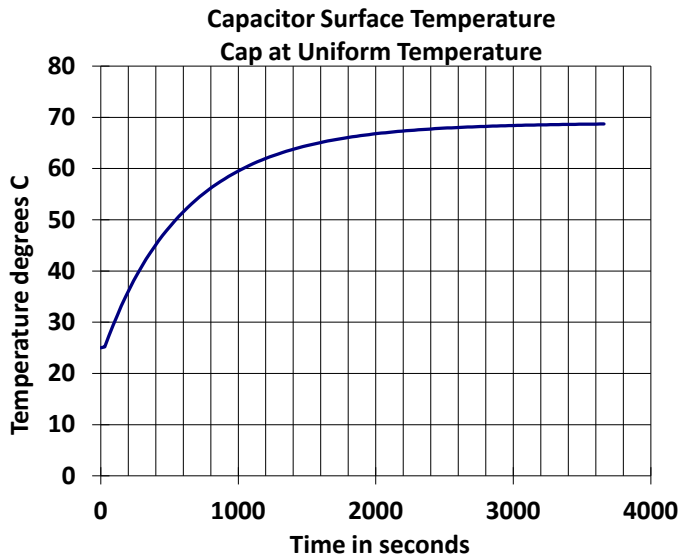
Sample 1.

Capacitor surface temperature rise above application environment @ 100 Amps RMS current load, 10 KHz.
Thermal resistance = 0.5°C/W:



Sample 2.

Capacitor surface temperature rise above application environment @ 100 Amps RMS current load, 10 KHz.
Thermal resistance = 1°C/W:



Mechanical Specifications

Dimensions:	Refer to layout details
Terminals:	Tin plated copper, 0.032" thick.
Encapsulation:	RTV case - UL 94-V0
Marking:	
SBE Inc.	SBE company identification
777D109	SBE "short form" part number
500 µF ±10%	Capacitance value and tolerance
700 Vdc	DC voltage rating
-40°C to +85°C	Operating Temperature Range
yyww-lot#-unit	12-digit serial number (date code, lot number, unit number)



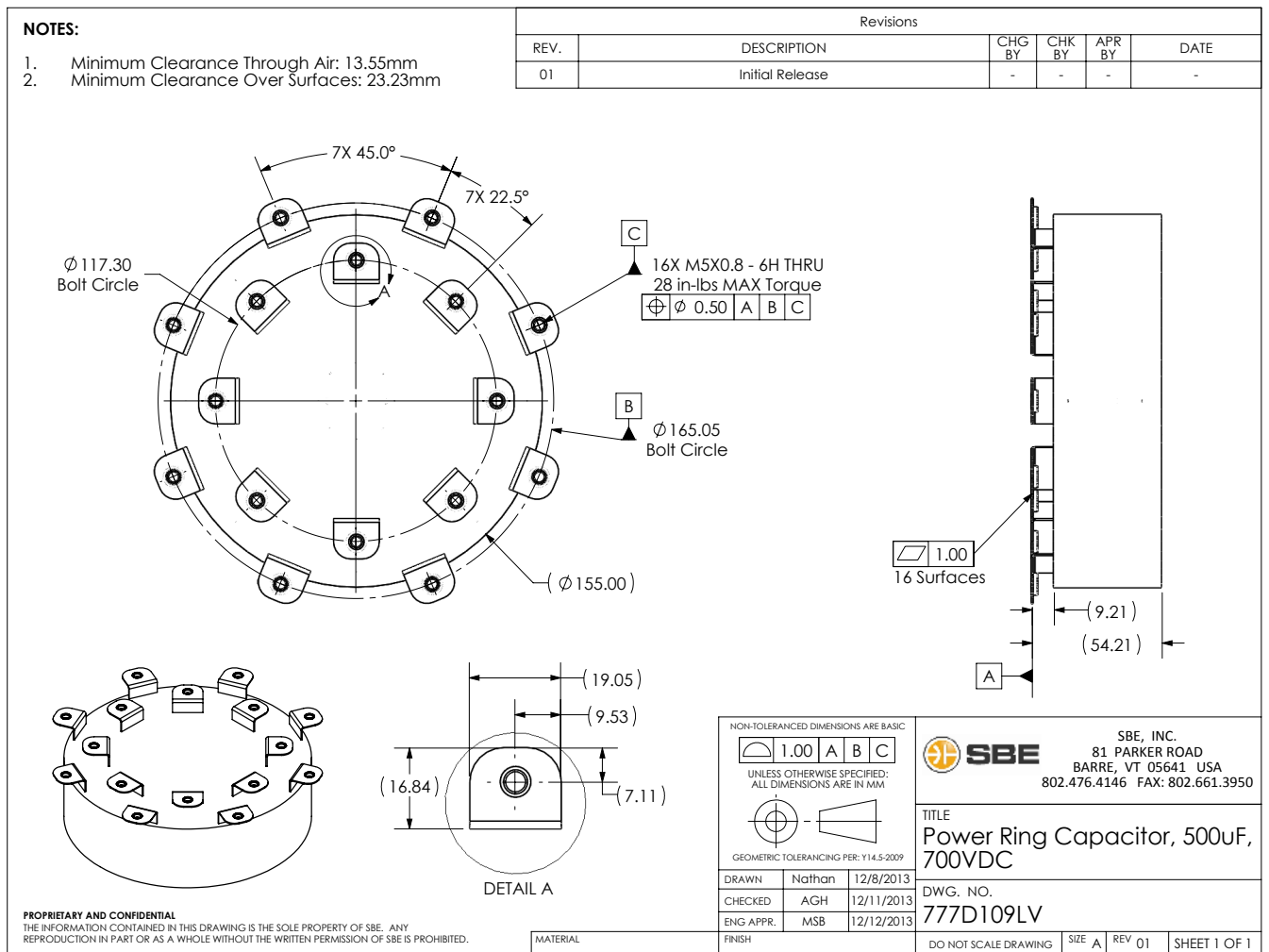
UL Recognition logo

Mechanical Mounting and Additional Thermal Notes:

This capacitor is optimized for extremely low self inductance when connected to a suitable laminar bus structure. The capacitor internal heating is VERY small, and other bus structure heat sources are very likely significantly higher than the heat added to the bus by the capacitor. Capacitor dissipation is approximately 4W at 100Arms, from 1-100KHz.

It is highly recommended to use infrared thermal imaging from a system cold start to determine the location and relative magnitude of thermal input to the bus. The capacitor may well function as a thermal conduit for bus structure heat, and it will be very possible that the capacitor internal hot spot is less than the terminal temperature. Thermal contour maps are available for some representative conditions.

Layout Details:



Contact SBE Inc. to discuss your specific requirements.

SBE reserves the right to amend design data

At the Leading Edge of Film Capacitor Technology®

Advantages of Power Ring DC Link Capacitors

- Ability to handle higher ripple currents with less capacitance, weight, and volume
- Service life of > 200,000 hours for realistic operating conditions, due to lower losses and better thermal performance
- Minimization of IGBT overshoot and elimination of the need for additional snubber capacitors
- Most effective isolation of DC storage or supply from AC switching artifacts
- Lowest industry ESL at <5nH typical with a properly integrated bus structure
- Smaller inverter packaging
- Overall system cost savings
- Capacitance from 400 μF to 2500 μF and voltages from 250 Vdc to 1200 Vdc

The SBE Power Ring Film Capacitors™ utilize traditionally available and economical polypropylene and polyester capacitor dielectric films. However, the *power of the shape™* allows for both thermal and electrical performance which has been unachievable in the film capacitor industry to date.

Power Ring System Performance

The combination of lowest available Trise, ESR and ESL coupled with highest ripple current handling capability enable the development of industry leading inverter designs with unbeatable performance and reliability.

Lowest available Trise for a given ripple current

Lowest available ESL, less than 5nH demonstrated with optimal integrated bus

Lowest available ESR, less than 150 micro-Ohms typical
Crown terminal architecture provides for a multitude of current paths which allows the monolithic capacitor to function as a distributed element with a much lower ESR than an equivalent array of smaller parts. SBE has developed a next generation capacitor simulation tool that allows accurate calculation of hotspot temperature to allow optimal rating with excellent reliability.

Integrating the Power Ring in an Existing Design

The “stacked” inverter design evolves from modifying a typical automotive inverter by utilizing the excess space left above the IGBT module (figure 1). By bending the end of the laminar bus plate, the IGBT, die, cooling plate, and the ring capacitor are “stacked” on top of each other in a symmetrical fashion. The ring capacitor is placed underneath the cooling plate. The cooling plate is shared with the IGBT module which is mounted on the top.

Figure 1

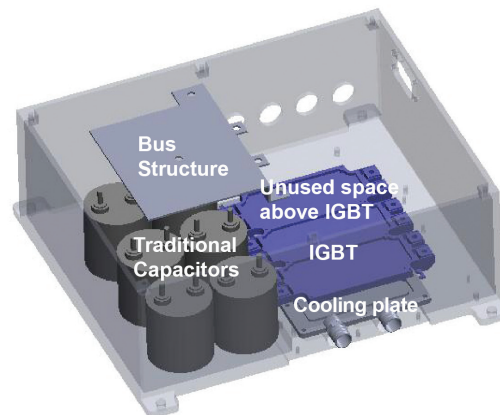


Figure 2

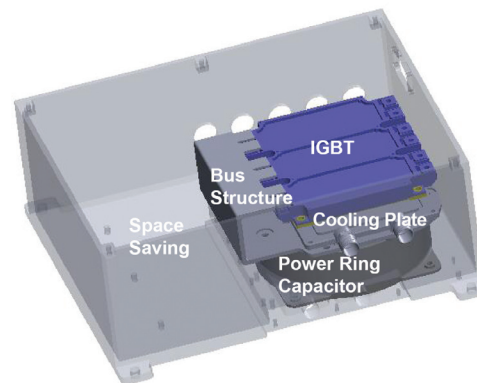


Figure 2 shows the “stacked” inverter design after the integration of the ring capacitor and the laminar bus plate. By now combining both aspects of vertical integration and the low temperature rise characteristics of the capacitors, an increase to 50% or more volume reduction is realistically possible. These improvements clearly translate into weight and cost reductions.

#SBE-PR-109-02/14